SARNOFF Corporation

CERAMIC/METAL COMPOSITE CIRCUIT-BOARD-LEVEL TECHNOLOGY FOR APPLICATION SPECIFIC ELECTRONIC MODULES (ASEMs)

Contract No.: DAAB07-94-C-C009

FINAL TECHNICAL REPORT

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Certificate of Technical Data Conformity

The David Sarnoff Research Center hereby certifies that, to the best of its knowledge and belief, the technical data delivered herewith under Contract No. DAAB07-94-C-C009 is complete, accurate, and complies with all requirements of the contract.

Date: 9/15/97

Certifying Official: _____

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TABLE OF CONTENTS

Executive Summary

The goal of this DARPA research contract, which began December 22, 1993, was to develop a board-level integration technology for fabrication of Application Specific Electronic Modules (ASEMs) for military systems. This technology will interconnect bare ICs, packaged ICs, and multichip modules (MCMs), as well as passive components on a single, high density interconnect board. To achieve this goal, the Sarnoff Corporation developed the LTCC-M (Low Temperature Cofired Ceramic on Metal) substrate technology and demonstrated its performance as a high density packaging technology for high speed digital, as well as RF and microwave military electronics. This technology is also suitable for fabricating hermetic single or multichip packages for a wide variety of military and hi-rel commercial applications. The combination of a low loss ceramic at microwave frequencies and a high conductivity metal core makes LTCC-M a natural choice for substrates and packages for advanced communication systems and mobile computing. Electrical feedthroughs in the metal core allow double-sided substrates to be fabricated with minimum interconnect length between the top and bottom sides of the circuit board. The LTCC-M circuit can also serve as "standardized" the power and ground planes for high density MCM-D signal layers. This reduces the number of MCM-D layers, resulting in a lower cost for such a module. Benzocyclobutene (BCB) test structures with thin film interconnects having nominal features sizes as small as 1 mil were fabricated on top of polished LTCC-M substrates to demonstrate this MCM-C/D capability. The LTCC-M substrate technology was successfully transferred to Dielectric Laboratories Inc. (Cazenovia, NY), who will be a merchant supplier of substrates and packages for commercial and military applications. During this program, four prototype circuits (each emphasizing a different attribute of LTCC-M) were designed and fabricated to prove out the technology. Three of these were completed and delivered to the supporting company as fully tested bare substrates. The performances of all of these substrates were favorably reviewed.

While the technology demonstration vehicles showcase qualities required for compact, high functionality military systems, they also support the creation of high volume products for the commercial marketplace. Typical military applications include: personal units for cellular communications systems and wireless LANS, electronics for tracking of military materials and components, construction of affordable broadband networks at military bases and installations, T/R modules for radar systems, and high power motor control systems. Specific military systems to which LTCC-M substrate technology can be applied include: Global Mobile Information Systems (US Army), "Total Asset Visibility," Power Electronic Building Blocks (US Navy), EKV Program (US Air Force), and the AEGIS Radar System (US Navy).

Materials System Highlights

Significant LTCC-M materials system accomplishments during this program include:

- Demonstrated the "**zero lateral shrinkage**" property of LTCC-M substrates
- Demonstrated (in situ fired) double-sided LTCC-M substrates, with electrical feedthroughs in the metal core; this was made possible by the "zero shrinkage" property of the LTCC-M technology.
- Demonstrated low loss, 50Ω transmission lines with seal ring feedthroughs; 50Ω lines were **tested to 20 GHz and exhibited low loss** (<0.25 dB/feedthrough, and <-15dB return loss) throughout this frequency range.
- Developed processing to form **high precision cavities (<1 mil tolerance)** in LTCC-M substrates.
- Temperature humidity studies at 85°C, 85%RH, 48 volts (>3000 hours) **show no evidence of silver migration** through the glass-ceramic, and demonstrate that the ceramic system fully densifies during firing.

- Daisy chain test structures have been fabricated in LTCC-M ceramic having 8 mil lines, spaces and vias. These test structures have undergone more than 250 thermal cycles between -40°C and +125°C, without any change in electrical resistance or any visible signs of via cracking.
- Development of a set of thick film materials that can produce high density substrates having 4 mil lines and spaces with 4 mil diameter vias in the ceramic; daisy chain structures have withstood **600 thermal cycles between -55°C and +125°C.**
- Five (5) patents were filed based on the LTCC-M technology developed under this research contract.

Technology Demonstration Vehicles

- 30 Optoelectronic Transceiver Packages were delivered to AMP for a 1.2Gbit/sec Fiber-in-the-Loop system. These packages were built with a **90% first pass yield**.
- 15 C-Band Power Amplifiers were delivered to Raytheon. The package was demonstrated to handle 38 dBm of output power at efficiencies greater than 45%, and **these amplifiers met or exceeded all specifications**.
- 350 Transposers for a 200 Watt power switch were delivered to Harris for the US Navy Power Electronic Building Block Program. These transposers demonstrated **very low inductive losses** as well as **excellent thermal conductivity**, critical properties for high power electronic modules.
- A Digital/RF Modem in 2-sided PCMCIA Card Format was also fabricated during this program. While no board passed bareboard test without any defects, it is expected that all problems can be readily fixed. **An important lesson learned from this task, is that the substrate design software must be developed for the substrate fabrication technology**. The incompatibility between design files and the substrate toolmaking software led to both errors and significant delays. This Technology Demonstration module also served the purpose of optimizing the electrical feedthrough process for the metal core.

Technology Transfer to a Merchant Supplier

An LTCC-M **Technology Transfer program was successfully completed with Dielectric Laboratories Inc.** (Cazenovia, NY). Dielectric Laboratories will be a merchant supplier of LTCC-M packages and substrates to both military and commercial electronics systems manufacturers. A goal of this program was to replicate the LTCC-M processing at Dielectric Laboratories and its chosen suppliers. **During this program all custom glasses, silver thick film inks, and green tape were transferred to commercial sources for scale-up to commodity sized lots**; the LTCC-M components were reformulated to account for differences of the purchased materials, and processing was adjusted to accept these changes. The Technology Transfer was concluded with the fabrication and delivery of 20 C-Band Power Amplifiers by Dielectric Laboratories.

In June 1997, DLI introduced LTCC-M technology to potential customers and to their reps at the IEEE MTTS show in Denver, CO. At this show, DLI also presented a paper on LTCC-M technology. This effort generated much interest from potential customers in the areas of high frequency and high thermal power applications. The aspect of low cost was also considered to be a technology driver. Since that time, DLI has had discussions with numerous potential customers such as Raytheon, AMP, Hughes, Litton, Alcatel and Ortel. Purchase orders from Raytheon, CTI, and Litton to build various packages have been received. DLI has submitted a quote to TRW to fabricate two MCMs for the DARPA Advanced Digital Receiver program.

DLI has prepared and distributed a capabilities brochure and preliminary design guideline for this technology. A WEB site is under construction to insure that information on this

technology is quickly and easily attainable. All LTCC-M manufacturing will be done in **a new 5000 square foot facility that has just been completed.**

Future System Extensions

The LTCC-M system will be extended to integrate passive components into the substrate under DARPA contract number F33615-96-2-5105. Materials to screen print capacitors and resistors on the LTCC-M green tape layers will be developed and transferred to Dielectric Laboratories Inc. Besides resistors and capacitors, inductors and filters can be formed within the substrate. Design kits, for both the LTCC-M technology (developed under the ASEM program) as well as the integrated passive components (developed under the Mixed Signal program), will also be developed to aid system designers in using this new substrate technology.

The large area capability of LTCC-M opens up new horizons for the use of ceramic substrates. Such areas include flat panel displays and phased array antennae where the control electronics are integrated with the display or antenna. A DARPA sponsored program is underway to develop and demonstrate technology for integrating electroluminescent displays with related electronics on high-performance circuit boards. In the long term, this technology forms a basic building block for supporting new display functionality by enabling the integration of sensors, communicators, processors, etc., onto the display panel.

Section I
Introduction

A. TECHNICAL PROBLEM

The electronics industry continues to require increased component packaging efficiency in order to achieve higher performance and reliability, while at the same time decreasing size weight and cost. Under this research contract, a board-level integration technology was developed for fabrication Application Specific Electronic Modules (ASEMs) for military systems. A board-level technology was selected in order to combine bare ICs, packaged ICs, and multichip modules (MCMs) on a single, high density interconnect board. To achieve high density and high reliability, requires a packaging technology that efficiently removes heat from high power density regions of the module.

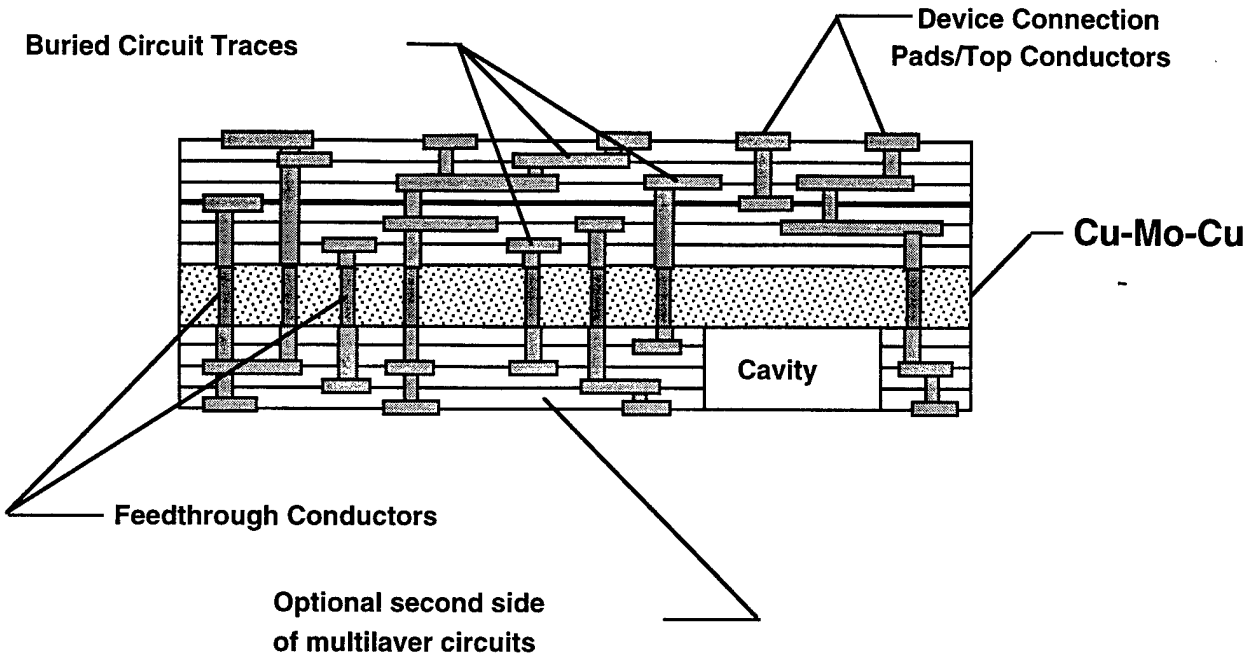


Figure I.1: Structure of an LTCC-M substrate with feedthroughs in the metal core

B. LTCC-M APPROACH

Under this research contract the Sarnoff Corporation demonstrated the LTCC-M (Low Temperature Cofired Ceramic on Metal) substrate technology as a high density packaging technology for high speed digital, as well as RF and microwave military electronics. This is schematically shown in Figure I.1. A key innovation of the LTCC-M approach, is the use of an integral (in situ fabricated) high conductivity metal core. This metal core combined with the process technology developed under this contract, allows multilayer ceramic circuits to be fired without any significant shrinkage in the x-y plane. The makes possible a large area, high yield, high density packaging technology. To achieve

the high reliability demanded by military electronics, a hermetic ceramic-on-metal system was designed to match the thermal expansion of GaAs, so that high power GaAs and silicon IC die could be directly mounted on LTCC-M packages. The LTCC-M packaging approach overcomes the traditional problems of small size and poor power dissipation of ceramic substrate technologies, as well as lower packing density and poor power dissipation of organic printed wiring boards.

C. TECHNOLOGY DEVELOPMENT TASKS

To demonstrate a board-level interconnect technology for advanced electronic modules, technology developments were required in the areas that follow.

Low Cost Feedthrough Process
- Hole fabrication by laser or mechanical drilling
- Hole insulation
- Center conductor

Green Tape Development
- Glass/ceramic
- Low loss ceramic
- CTE of glass/ceramic matched to Cu/Mo/Cu
- Green tape formulation

Ceramic to Metal Bonding
- Cu/Mo/Cu surface preparation
- Glaze development
- "Zero" lateral shrinkage

Conductor Development
- Buried silver conductor
- Via silver conductor
- Exposed Ag/AgPd conductors

Multilayer Integration
- Double-sided board fabrication and firing
- Precision cavity formation process

Thin Film Process
- Thin film conductors on glass/ceramic
- BCB processing
- Thin film multilayers on LTCC-M

This research program was designed so that most of the above developments were demonstrated during the initial phase of this program. Phase 1 concluded with the fabrication of a test structure, which was then subjected a series of reliability tests.

Following the demonstrations of these technology elements, the LTCC-M technology was transferred to a merchant supplier of packages and substrates, Dielectric Laboratories, Inc. (Cazenovia, NY) during Phase 2. To validate the LTCC-M technology, four Technology Demonstration Vehicles were selected to be designed and fabricated during this program phase. These were:

- C-Band Power Amplifier (in cooperation with Raytheon Corp.)

- Optoelectronic Transceiver Package (in cooperation with AMP Inc.)
- RF Modem with Digital Processor in PCMCIA format (in cooperation with Torrey Science Corp.)
- Power Electronic Building Block "lid" (in cooperation with Harris Corp.).

Section II
LTCC-M Materials System

To facilitate the transition to manufacturing, the LTCC-M packaging technology was expressly designed to be compatible with the already existing infrastructure for cofired ceramic substrates and packages. The primary LTCC-M manufacturing processes are shown in flowchart form in Figure II.1. The metal preparation processing is the only major departure from standard cofired ceramic technology.

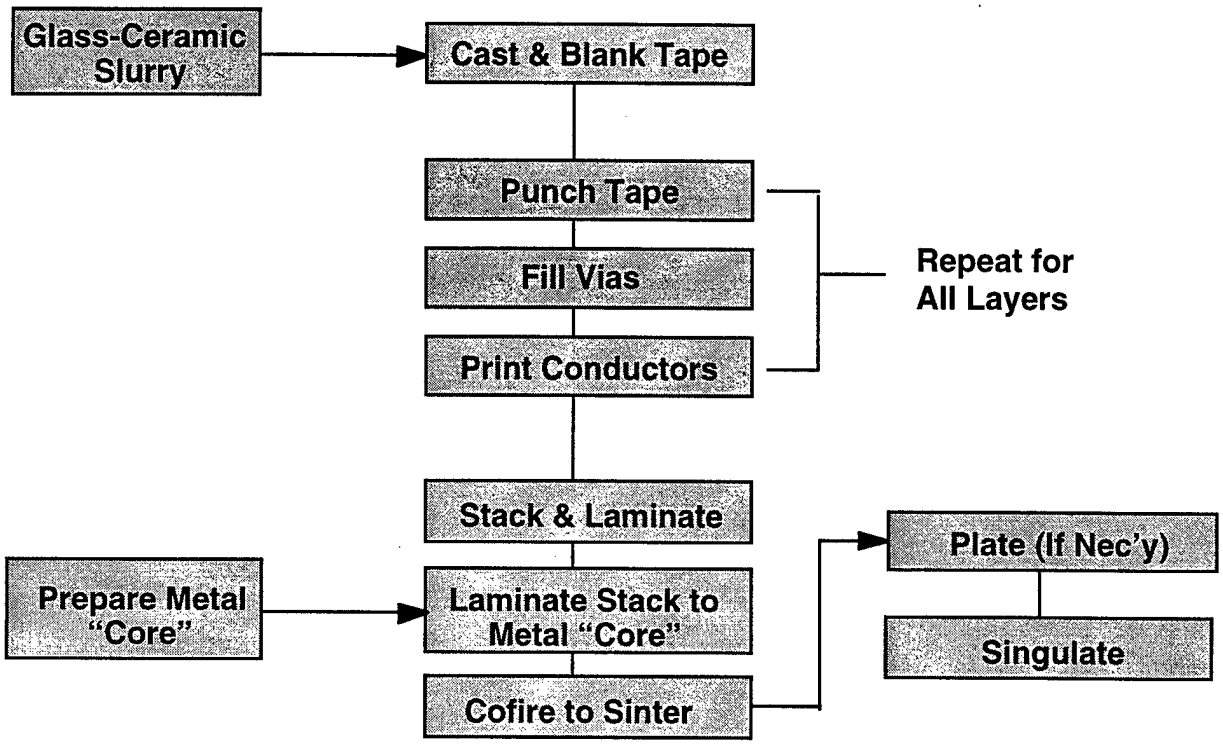


Figure II.1: LTCC-M process flow for fabrication a typical package.

A. COPPER/MOLYBDENUM/COPPER BASE

The metal base is the foundation upon which the LTCC-M structure is built. All ceramic layers must be matched to the metal base, and the metal base must be compatible with all processing steps. Since the LTCC-M package must allow direct attachment of bare GaAs and Si ICs, as well as provide a high thermal conductivity path for heat removal from these chips, a 13/74/13 Cu/Mo/Cu tri-layer laminate from CSM Industries (Cleveland, OH) was chosen. This material is well matched to GaAs (thermal expansion about 6 ppm/°C), offers a high thermal conductivity (x,y = 210 W/(m-°C), z = 170 W/(m-°C)) comparable to aluminum or aluminum nitride. Since it is far less expensive than large area AlN substrates, it offers the best compromise between cost and performance.

The LTCC-M system is designed to be fired at about 900°C in a standard conveyor belt furnace with an air atmosphere. To protect the Cu and the Mo from this harsh environment, the metal core is Ni plated (about 1 mil thick) in a

sulfamate Ni electrolytic plating bath. The Ni oxide that is formed during the high temperature operations is well adhered to the metal core, but can be removed (if desired) by subsequent chemical operations.

B. GLASS/CERAMIC

In the LTCC-M system, glass/ceramic in the form of green tape is fired onto a metal core. The glass/ceramic system is designed to have excellent dielectric properties, in addition to being well matched in thermal expansion to the Cu/Mo/Cu metal core. The LTCC-M packaging technology is intended for modules spanning the range from high speed digital applications to microwave transmit/receive applications. Therefore, only materials exhibiting good dielectric performance at frequencies of 15 - 20 GHz qualified for further evaluation. To demonstrate good dielectric properties in this frequency range, the glass/ceramic is designed to be fully crystallized and contain only a very small amount remnant glass. Excess remnant glass will lead to high dielectric loss at the X-band frequency range.

We chose to investigate the MgO-SiO_2-Al_2O_3 phase diagram for candidate materials. Glass compositions were discovered which fully crystallize when fired at about 900°C for 30 minutes. After investigation of a great many custom-melted glasses from this phase diagram, glass compositions were found that principally crystallize cordierite and forsterite. Both of these crystals are known to exhibit excellent dielectric properties at microwave frequencies. By varying the relative proportion of each of these crystals in the fired glass ceramic, one can control its thermal expansion properties. Proper mixing of these glasses allows one to design glass/ceramic compositions that when fired at 850 - 950°C, will match the thermal expansion characteristics of the Cu/Mo/Cu base.

When green tape made with this glass/ceramic formulation is fired (at 900°C) onto the Cu/Mo/Cu base, using a specially formulated bonding glaze, essentially **zero lateral (x-y) shrinkage is observed in the fully densified ceramic structure**. The bonding glaze is fired onto the Cu/Mo/Cu base prior to the lamination of the green tape stack onto the metal base. **The LTCC-M parts are fired as free standing structures, without the aid of weights or fixtures.**

C. THICK FILM CONDUCTORS

Each layer of green tape has a screen printed conductor pattern that is connected to adjacent layers by conducting vias in the tape. During the course of this program, a number of thick film conductor inks were formulated for specific purposes. These inks were as follows:

- silver ink for buried conductor traces
- silver ink for top layer conductor features
- silver-palladium (30%) for top conductor features
- silver contact pad for the Cu/Mo/Cu core
- silver via fill ink
- silver via fill ink for the Cu/Mo/Cu core feedthroughs
- gold via fill ink for the Cu/Mo/Cu core feedthroughs
- fine line silver conductor inks
- small via fill inks

The LTCC-M packaging system was designed for use in high volume commercial electronics markets. Therefore, a silver conductor system was chosen to minimize materials and processing costs. The conductor inks were designed for printing conductors with 8 mil wide lines and spaces. The buried conductor inks are fritless and are formulated using silver flake materials. The buried silver conductors exhibit a surface resistivity of about 4 mΩ/square. To develop good adhesion to the ceramic, the top conductors contain some glass added to their formulations, and the silver top conductor exhibits a surface resistivity of about 7 mΩ/square. Top conductors can be subsequently plated with Ni/Au layers (using electrolytic or electroless baths). These conductors were printed using 290 mesh, 0.8 mil diameter, special high strength alloy screens, having 0.7 -1.0 mil thick emulsions. The fine line silver inks were demonstrated below 4 mil wide lines and spaces. The inks were printed through 400 mesh stainless steel screens having 0.5 mil thick emulsions.

The standard vias used during this program were 8 mil in diameter. No capture pads are required, thus the per layer routing density is greatly increased. These vias were filled by screen printing techniques using 2 mil thick stainless steel stencils having 9 mil diameter holes. Special small diameter via fill inks were designed for filling 4 mil diameter vias using a an injection via fill machine from Pacific Trinetics.

D. METAL CORE FEEDTHROUGH SYSTEM

The development of a technology to fabricate many small electrical feedthroughs within the metal core is one of the central features of the Phase I research program. To obtain high reliability, the insulator in the hole must match the thermal expansion of the metal core (13/74/13 Cu/Mo/Cu). Most work was concentrated on the fabrication of 13 mil diameter electrical feedthroughs, the smallest standard plated-through hole used by the printed wiring board industry. Smaller feedthroughs are possible using laser drilled holes in the metal core.

The basic feedthrough fabrication process involves opening up a hole (e.g. drilling and deburring), applying a layer of nickel to seal the molybdenum, depositing an annular ring of insulation in the hole, and finally depositing a conductor in the center core of the insulator. The conductor and insulator must be able to withstand the 900°C firing step required to complete the LTCC-M fabrication process. For high module yields the insulator must be deposited above a minimum thickness and not contain pinholes. After the hole has been formed, an insulating ring must be deposited, and finally the center conductor filled. Many insulator deposition techniques were investigated, and screen printing emerged as the best solution for mass production of electrical feedthroughs in the metal core. In this report, the suction screen printing process will be described, and data will be presented showing the reliability of this process.

Hole Fabrication

Holes in the Copper/Molybdenum/Copper (Cu/Mo/Cu) metal core were formed using standard numerically controlled, mechanical drilling machines. The focus of the work was to drill 13 mil diameter holes and then deburr using a

soft stone. This produced holes having sharp corners. These sharp corners were chamfered using a small diameter center drill. It was also noted, that it was significantly more difficult to drill 13 mil holes in 40 mil thick Cu/Mo/Cu, compared to drilling 20 mil thick metal cores. After deburring, these holes are Ni-plated by electrolytic methods. Cross sections (shown later in this report) show the Ni-plate to be quite uniform in the hole.

Experiments were also performed using a laser to drill holes in Cu/Mo/Cu metal cores. Holes were drilled by Coherent General (Sturbridge, MA) using a Nd:YAG laser at 15-30 watts, with 0.6 msec. pulse lengths. 13 mil diameter holes could be readily drilled in both 20 and 40 mil thick Cu/Mo/Cu. The minimum hole diameter was 7 mils for 20 mil thick Cu/Mo/Cu and 8 mils for 40 mil Cu/Mo/Cu. After drilling a "slag" residue remained around the perimeter of the laser drilled holes, this could be removed by mechanical means. However , it was decided to pursue mechanical drilling because it offered much faster turn-around times.

Electrical Feedthrough Insulator

The glass insulator of the metal core feedthrough is one of the critical materials required for development of a high yield manufacturing process for 2-sided LTCC-M substrates. The insulator must exhibit the following quantities:

- Good wetting at the glass/metal interface
- High adhesion to the metal core
- Compatibility between center conductor, glass insulator, and metal core
- Stability through subsequent LTCC-M firing steps

The insulation scheme for this feedthrough relies on multiple layers of dielectric insulation, as illustrated in Figure II.2. Thus, a defect in a single layer will not readily propagate through the entire insulator, causing a manufacturing defect (i.e., "shorted" feedthrough). As shown in Figure II.2, the Ni-plating on the metal core is first oxidized at 820°C, producing a tough, uniform oxide layer that exhibits resistance of 10^8 - 10^9 Ω. On top of this, multiple layers of insulating glass are deposited and fired.

A large number of glasses were surveyed. These included both vitreous and crystallizing glasses. A glass formulation, designated G-14, has been chosen as the insulating glass. The thermal expansion of this glass is well matched to Mo (CTE ~ 5 ppm/°C). G-14 is a crystallizing glass, and x-ray diffraction measurements indicate that willemite forms above 800°C.

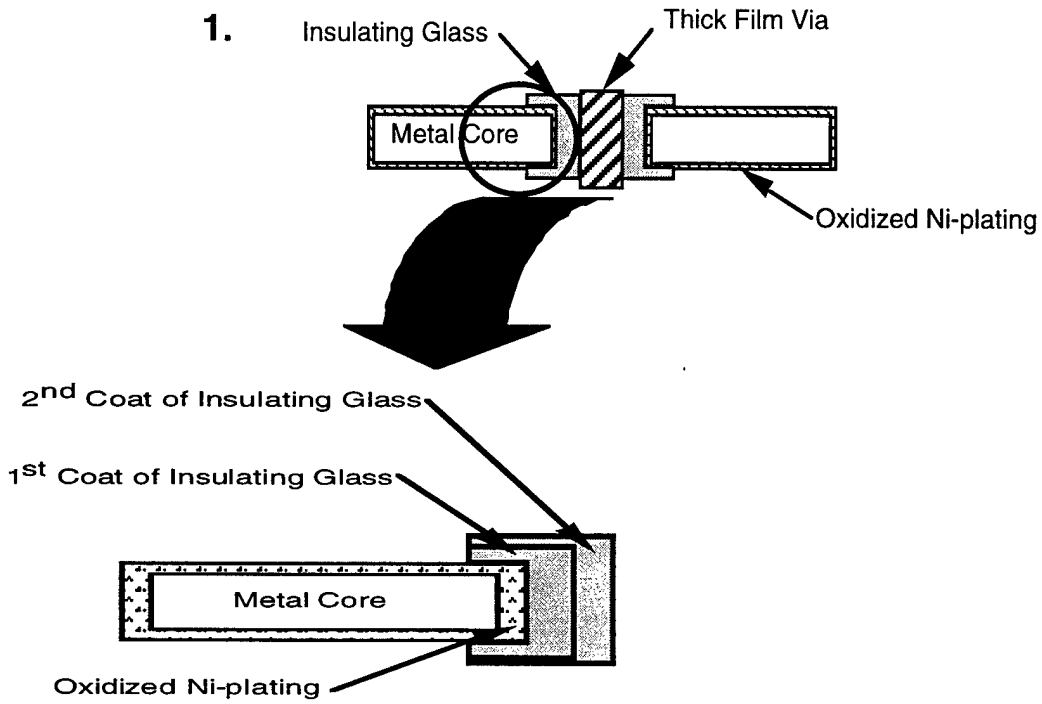


Figure II.2: Feedthrough insulation scheme using multiple layers of insulation.

During the course of this work, it was decided that use of a suction screen printing process would be the best way to produce a large number of reliable feedthroughs in the metal core with a high manufacturing yield in a cost effective manner. Furthermore, this process does not require any additional equipment beyond what is required for the standard LTCC-M process.

The steps in the suction screen printing process are illustrated in Figure II.3. First, a dielectric thick film paste (of appropriate rheology) is screen printed over the hole. After the screen printer squeegee has completed its stroke, a vacuum is applied underneath the metal core, to suck the dielectric ink down the hole forming an annular ring. The part can then be removed from the screen printer for drying. To produce an insulating pad, as shown in Figures II.4 and II.5, after firing in air the metal core was turned over and suction printed on the bottom side and fired again using a standard thick film firing profile. This process can be repeated if additional coats of insulation are desired. Finally, the thick film silver center conductor is deposited using standard via fill screen printing techniques. To form a capture pad on both sides of the metal core, after drying the metal core can be turned over and printed before firing.

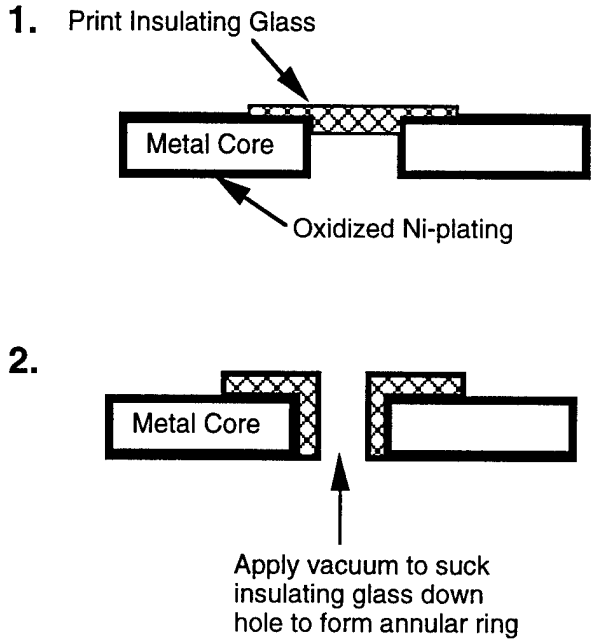
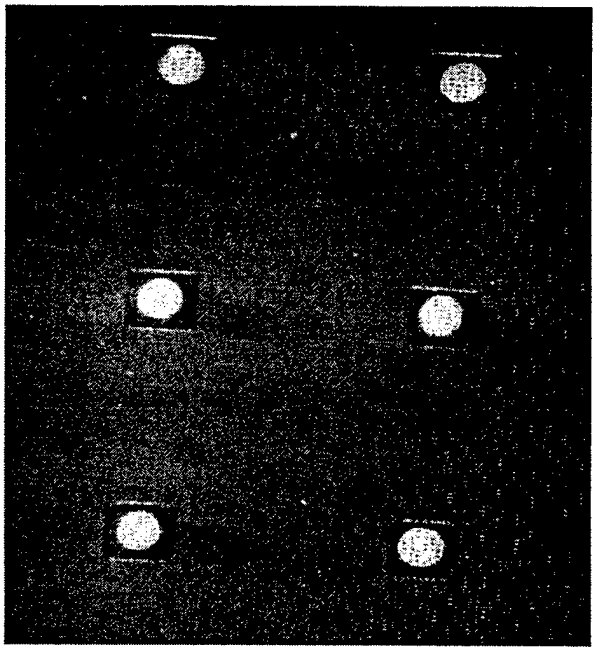


Figure II.3: Schematic illustration of suction screen printing of insulation.



FigureII.4: Group of electrical feedthroughs in a Cu/Mo/Cu core on 200 mil centers

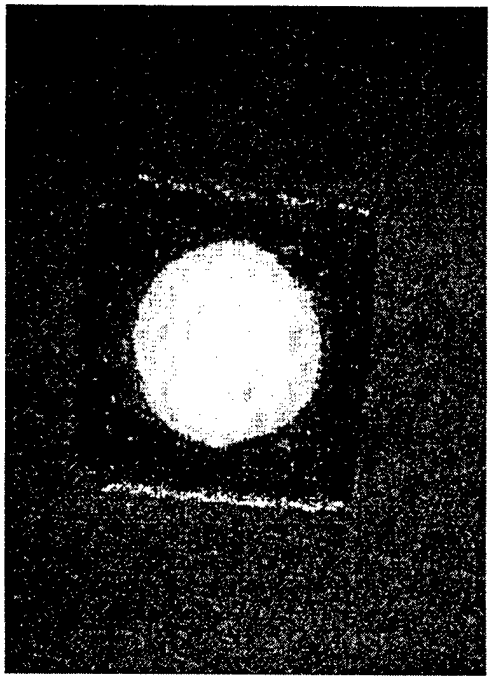


Figure II.5: Enlarged view of an electrical feedthrough with a 50 mil square insulating pad and a 30 mil diameter contact pad

The basic feedthrough process steps are summarized in Figure II.6. A cross section of a 13 mil diameter electrical feedthrough in a 20 mil thick Cu/Mo/Cu metal core is shown in Figure II.7. Figure II.8 shows a scanning electron micrograph of a portion of the cross-section of Figure II.7. These figures show that the electrical feedthrough materials system components are quite compatible with each other. In particular, the glass/metal interfaces show excellent wetting characteristics, required for high yield processing.

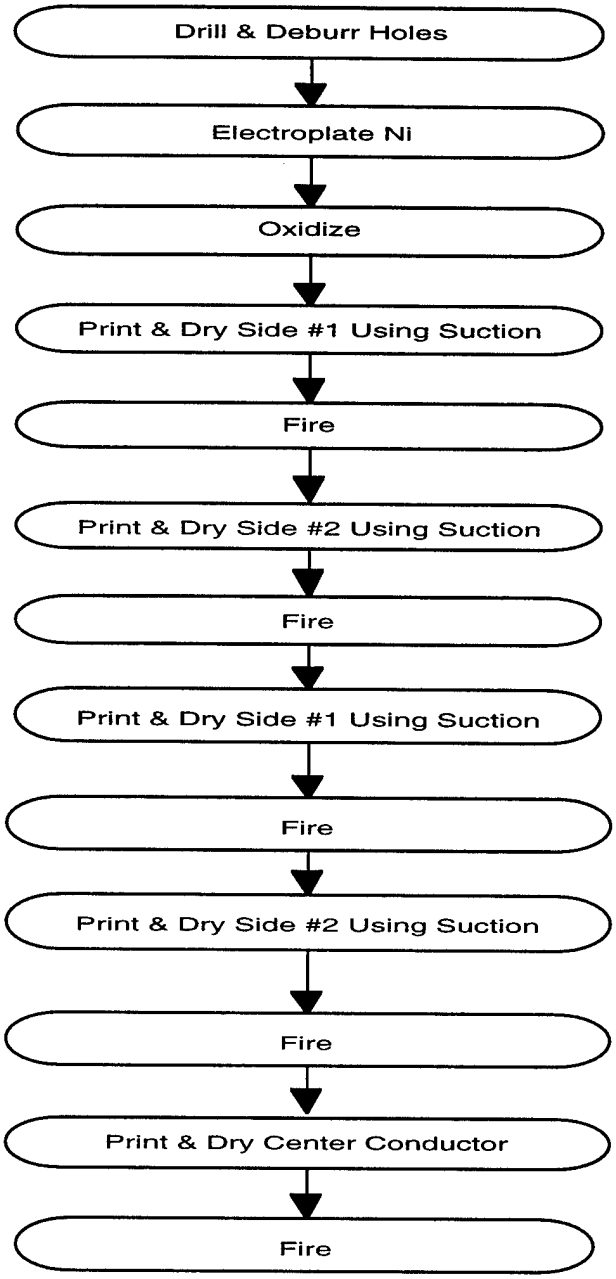


Figure II.6: Process steps for the mass fabrication of electrical feedthroughs in a Cu/Mo/Cu core.

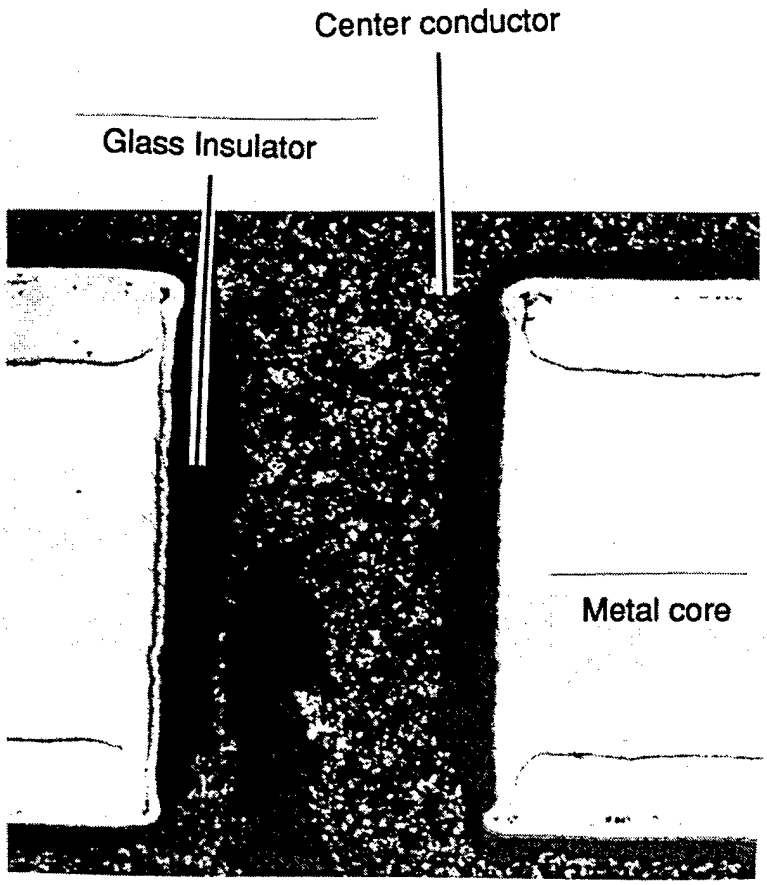


Figure II.7: Cross section of a 13 mil diameter feedthrough in a 20 mil thick Cu/Mo/Cu metal core

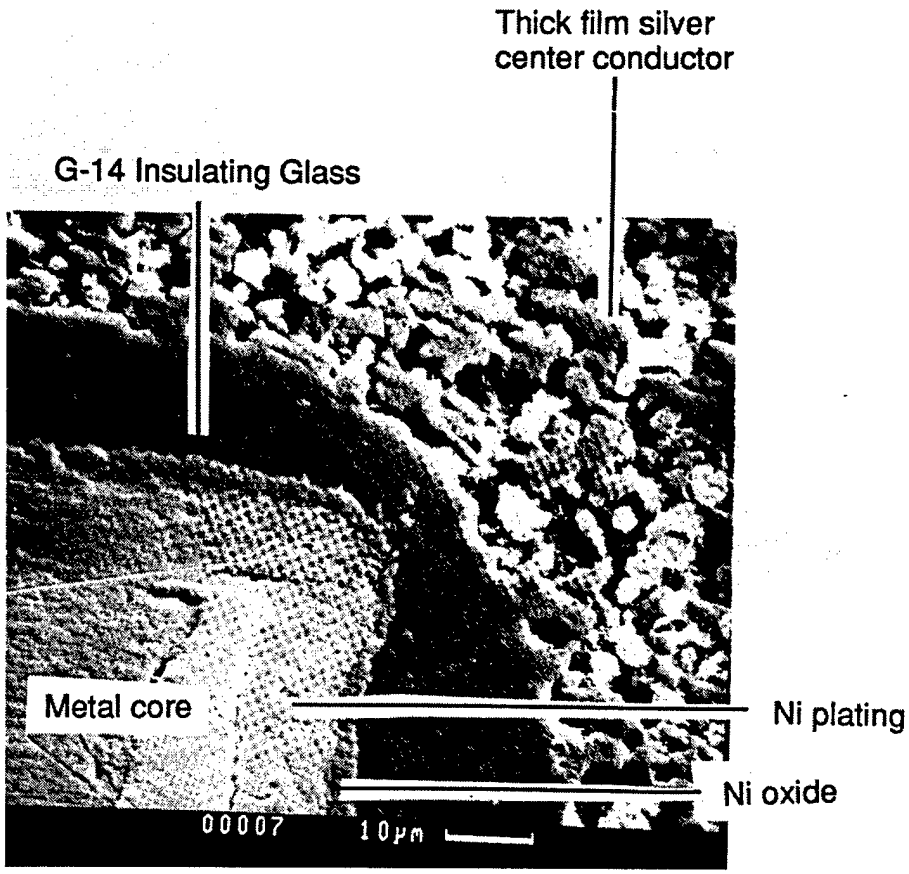


Figure II.8: Scanning Electron Micrograph of an electrical feedthrough in Cu/Mo/Cu metal core

Electrical Feedthrough Center Conductor

The primary requirements that the center conductor must meet are as follows:

- good electrical conductivity
- low cost metallurgy
- compatibility with insulator and metal core
- reheat stability for subsequent firing process steps
- compatibility with LTCC-M materials
- complete filling of central area

For nearly the entire research effort, the center conductor was a silver thick film ink designed for filling using standard thick film via filling techniques. The thick film ink contains the following components:

- silver powder
- crystallizing glass G-14
- organic vehicle

The leakage resistance of the feedthroughs described above is approximately $10^9\Omega$.

Gold Feedthrough Conductors

The Advanced PCMCIA Card Technology Demonstration Vehicle taught a valuable lesson. While this substrate only had 19 feedthroughs in a 2.5" x 4.3" metal core, the insulators around these feedthroughs exhibited a much greater tendency to form fine cracks than any of the more complex reliability test structures (204 feedthroughs in a 2.5" x 2.5" area). During the cofiring process for this double-sided module, some of these feedthroughs developed high resistance shorts (1kΩ - 10MΩ) to the metal core. It was suspected that this was due to silver movement along the fine cracks during the firing operation. Since gold does not exhibit this migration phenomenon, gold inks were formulated for forming the feedthrough center conductors. These gold inks were formulated by simply replacing the silver powder with gold powder, and adjusting the resin content to obtain the proper rheology for filling the feedthroughs. Substrates in the format of the Advanced PCMCIA Card were fabricated (and having a high density of fine cracks in the insulator glass), without a single short to the metal core being observed with the gold feedthrough conductors.

E. BCB THIN FILM OVERLAY FOR LTCC-M

The objective of this portion of the program was to demonstrate that MCM-D interconnect structures can be built on top of LTCC-M ceramic substrates. This was accomplished by the fabricating a multi-level, thin film interconnect structure and subjecting this structure to the relevant reliability tests. A non-photosensitive BCB (Cyclotene™) from Dow Corning was chosen as the MCM-D technology.

The following processing sequence was used for thin film interconnect fabrication:

(a) Capture pad and first -level metal definition

1. Sputter Ti-Cu seed layer (1500Å Cu)
2. Apply photoresist, Expose 1st. level of thin film, and develop
3. Electroplate Copper (5 μm) through resist openings
4. Remove resist
5. Remove TiCu seed layer by ion milling

(b) Via pattern definition

6. Spin Apply adhesion promoter and Cyclotene™ 3022-57
7. Cure in flowing nitrogen at 250°C for 1 hour
8. Sputter 2000Å Cu as a mask
9. Apply photoresist, expose via pattern and develop
10. Wet etch copper ($FeCl_3$) through exposed resist to define via mask
11. Plasma Etch vias in Cyclotene™
12. Strip Cu mask in $FeCl_3$

(c) Top metal and via deposition:

13. Sputter TiCu seed for top metal
14. Apply photoresist, expose top metal pattern and develop resist
15. Electroplate top metal Cu-Ni-Au
16. Remove seed layer of Ti-Cu by ion-beam milling

Substrate polishing:

LTCC-M substrates were found to be easy to polish to very high surface finish (~150Å CLA) to obtain a nearly pore-free surface for thin film fabrication. The camber of the substrates was low so that the planarization during polishing could be contained within one layer (0.004") of ceramic on the 2.5" x 2.5" parts. The glass-laden silver vias were found to be well adhered to the ceramic walls, and showed no cracking, separation, pits etc. in the polished parts. The nickel-plated Cu/Mo/Cu cores held up well to thermal processing steps in the process. Concerns have been raised regarding the differential heating of the metal core in plasma ashers and etchers used in the process. While no such problems ever materialized, it is felt these concerns can be alleviated by ashing in the so-called down-stream ashers where the sample is exposed to the plasma outside the RF field.

Thin Film Test Structures:

Two types of thin film test structures were designed, to match up with two types of ceramic test vehicles that were built to evaluate reliability. Both these test vehicles consisted of two levels of thin film wiring, one level right on the polished ceramic surface and another on top of the BCB dielectric layer. Vias of 25, 50 and 75 μm diameters interconnected the thin film wiring in the two levels. The structure was also interspersed with fully testable, dense thin film wiring (thin film lines of 25 μm lines/50 μm pitch, 50 μm lines/100 μm pitch), to obtain an estimate of interconnect yields.

Another aspect of the test vehicles was that they yielded many fully testable via daisy chains consisting of thick film silver lines in the ceramic, thick film via to thin film capture pad interfaces, and thin film wiring on two levels of the structure. These were electrically characterized initially and after temperature cycling for yield and reliability assessments. The results, discussed in another part of this report, showed that the thin film interconnects can be fabricated on the LTCC-M substrates at high yields, and that these structures were highly reliable.

F. SUMMARY OF LTCC-M MATERIAL PROPERTIES

Physical Properties

Physical Properties of the Metal Core

Coefficient of thermal expansion Cu/Mo/Cu (13/74/13 ratio)	55 x 10^{-7}/°C
Thermal conductivity Lateral (x-y plane) Through thickness (z)	 210 W/m-°C 170 W/m-°C
Core thickness	5 to 40 mils

Physical Properties of the Ceramic

Firing temperature	875 - 925°C
Dielectric constant @10 KHz (25°C) @15 GHz (25°C)	 5.6 5.5
Dielectric loss @15 GHz	 0.001
Volume resistivity	5 x 10^{15} ohm-cm (25°C)
Thermal coefficient of expansion	56 x 10^{-7}/°C (25 to 400°C)

Ceramic-on-Metal

Substrate camber	0.002"/"
x, y shrinkage	0±0.1%
Z-directional shrinkage	40±10%
Surface roughness	
As fired	400 - 600 nm CLA
After polishing	150 nm CLA
Conductor	
Inner layers	Thick film silver
Surface layer	Thick film Ag with plated Ni and Au or thick film AgPd
Sheet resistance	3 - 5 milliohms/sq.
Wirebondability (Au thermosonic)	Good
Number of layers	15 demonstrated (more possible)
Green sheet thickness	200 μm
Fired sheet thickness	125 μm
Line resolution	
Line width	100 μm
Line spacing	100 μm
Via diameter	200 μm
Via pitch	600 μm
Substrate size	10" x 10"- projected

Note: Via diameters of 100 μm and pitches of 300μ can be achieved in low volume production

Microwave Properties

Figure II.9 shows a test structure designed to study 50Ω transmission lines and their transitions through a package seal ring. The transmission line is a microstrip line over most of its length, except in the region where it passes under the ceramic seal ring wall, where it is a narrowed stripline for impedance

matching. The transition between these two regions is slightly tapered to minimize the effects of green tape layer misalignment.

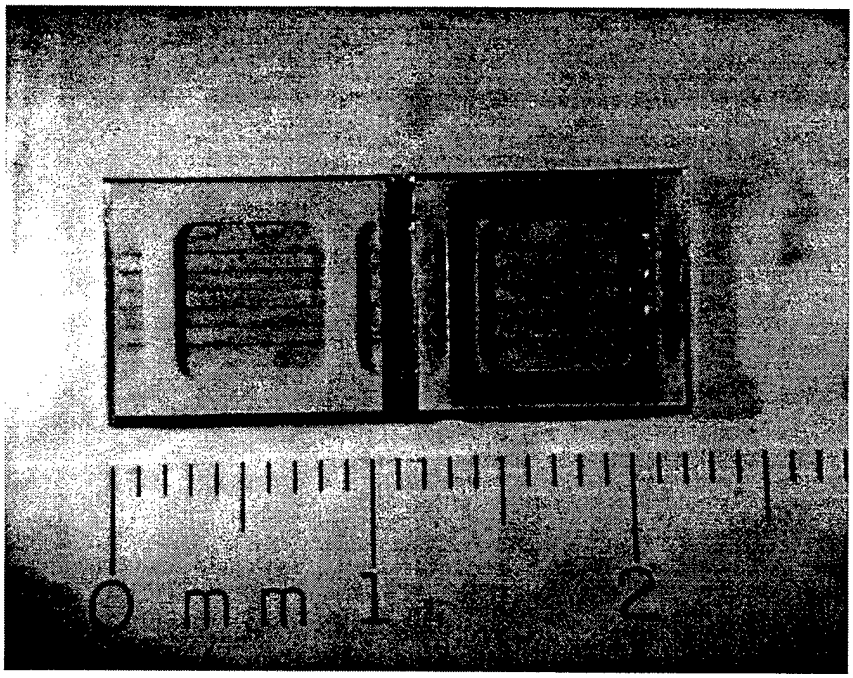


Figure II.9: LTCC-M package test structure built with 50Ω evaluation transmission lines having graded dog-bone transitions into the package.

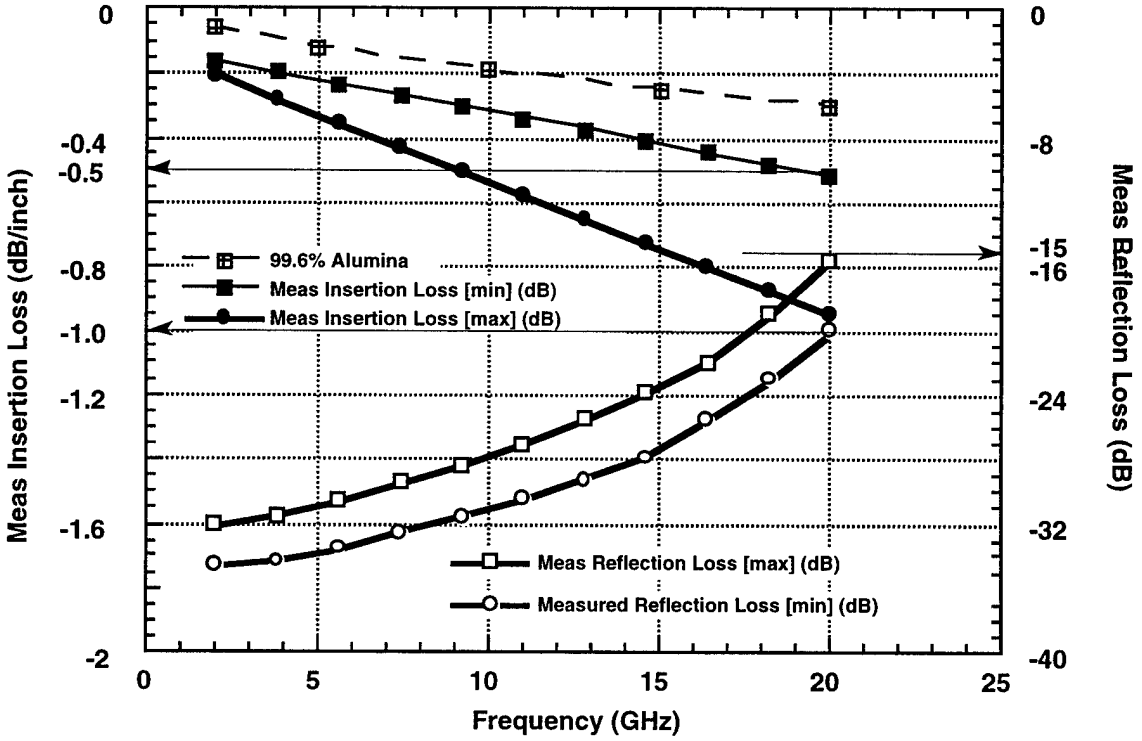


Figure II.10: Measured insertion and reflection loss for the LTCC-M package test structure.

Figure II.10 shows the results of de-embedded S-parameter measurements made using a HP8510 vector network analyzer and a universal launch test fixture. The range of values shown in Figure II.10 for each case is due to the variation in fixturing for the measurement of multiple devices. The maximum insertion loss is less than 1 dB/inch up to 20 GHz and the maximum reflection loss is less that -15 dB up to 20 GHz.

The screen printed nature of the LTCC-M technology and its low cost per square inch make it attractive for integrating microstrip components such as transformers, filters, couplers, and discrete inductors directly into the package.

Section III
Phase I Reliability Testing

A. TEST STRUCTURES

During Phase 1 of this research contract, a daisy chain test structure was designed to test the LTCC-M fabrication processes. Figure III.1 is a cross section of a test coupon having standardized daisy chains on both sides. Single-sided test structures use only the top side pattern, and do not have any feedthroughs in the metal core.

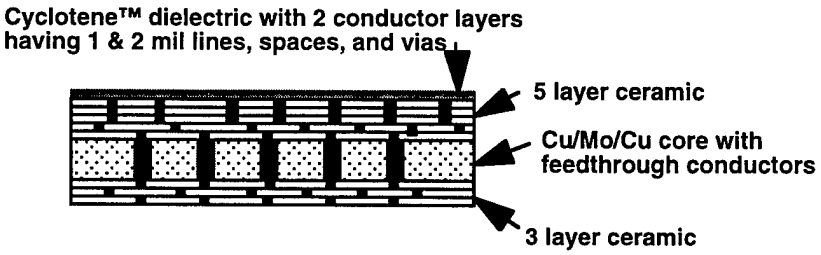


Figure III.1: High density test structure fabricated to demonstrate the integrity of the LTCC-M materials system.

1-sided Test Structures

The initial structures were fabricated as 1-sided test boards having 4 interconnected LTCC-M layers, without the Cyclotene™ thin film overlay. The general daisy chain structure (all layers combined) is shown in Figure III.2. This figure shows that 9 chains are produced from each sample. The daisy chains demonstrate high, medium, and low density structures in the LTCC-M circuit board. Some details of the pattern are shown in Table III.1.

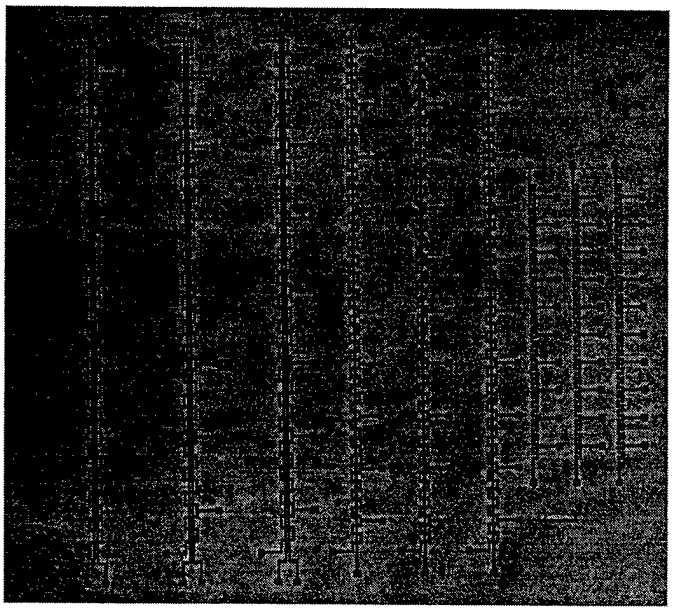


Figure III.2: Composite of all 4 thick film layers of the LTCC-M daisy chain pattern.

Layout Statistics
1-sided Test Structures

- **4 layer daisy chain pattern**
- **9 daisy chains interconnecting a total 978 vias**
- **High density via region:**
  - **No lines between vias**
  - **8 mil diameter vias on 16 mil centers**
  - **120 vias/chain**
- **Medium density region:**
  - **8 mil vias on 30 mil centers**
  - **Allows 1 circuit trace line (8 mil line/7 mil space) between vias**
  - **120 vias/chain**
- **Low density region:**
  - **8 mil vias on 42 mil centers**
  - **Allows 2 circuit trace lines (8 mil line/6 mil space) between vias**
  - **84 vias/chain**

Table III.1

After fabrication, these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit any degradation (data is shown later in this section).

2-sided Test Structures

Next, 2-sided test structures were fabricated on a metal core having electrical feedthroughs using the same basic test pattern. However, the top of the board had three layers (layers #1-3), and the bottom of the board had the fourth layer (and 2 additional layers for handling integrity). The electrical feedthroughs in the Cu/Mo/Cu core connected layer #3 on the topside to layer #4 on the bottomside. The electrical feedthroughs were mechanically drilled, which limits their density to only connect the medium and low density areas of the test pattern. Therefore, only 6 daisy chains were interconnected on the 2-sided test structures. The details of the 2-sided test structures without thin film overlays are shown below in Table III.2.

Layout Statistics 2-sided Test Structure (LTCC-M only)
•4 layer daisy chain pattern
•Cu/Mo/Cu has 204 13 mil diameter electrical feedthroughs
•6 daisy chains interconnecting a total 822 vias in the ceramic
•Medium density region: 8 mil vias on 30 mil centers Allows 1 circuit trace line (8 mil line/7 mil space) between vias 120 vias + 40 feedthroughs/chain
•Low density region: 8 mil vias on 42 mil centers Allows 2 circuit trace lines (8 mil line/6 mil space) between vias 84 vias + 28 feedthroughs/chain

Table III.2

After fabrication these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit any degradation (data is shown later in this section).

Low Density Test Structures with thin film BCB polymer overlays

A 36-hole/layer (a 6 x 6 matrix of 8 mil vias on 200 mil centers) test pattern was used to develop the processing for adding BCB polymer overlays to LTCC-M ceramic circuits. The test structures were 1-sided circuit boards fabricated with 4 layers of interconnected vias in the ceramic, and 2 conductor layers of thin film conductors connected together in daisy chain fashion. One of the thin film test structures is shown in Figure III.3. The details of these test structures are shown below in Table III.3.

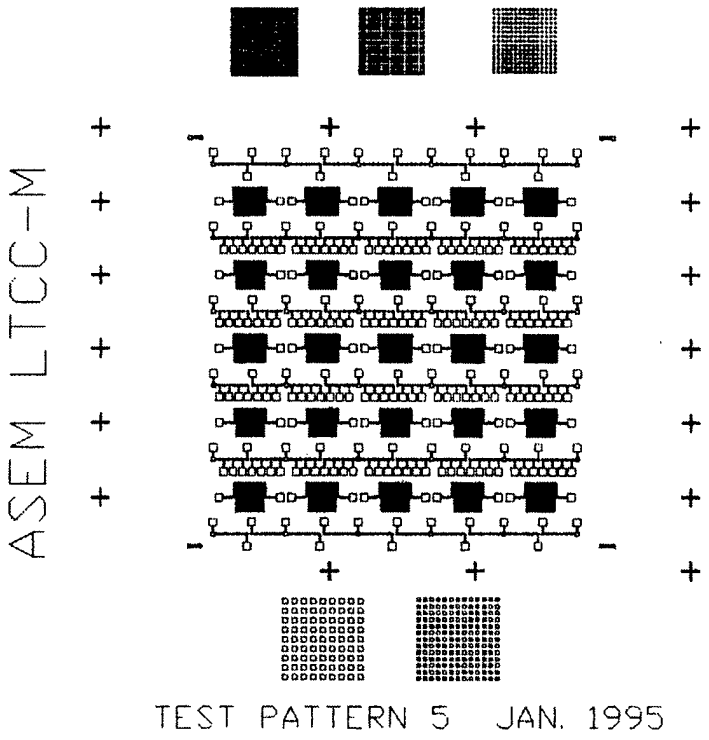


Figure III.3: Low density thin film test pattern for LTCC-M

Layout Statistics

low density pattern with BCB overlay

- **2 level BCB daisy chain**
  - **1 and 2 mil lines, spaces, and vias**
  - **3 mil diameter capture vias to ceramic vias**
  - **508 thin film vias**
  - **25 1 and 2 mil wide meander line patterns**
- **4 layers of LTCC-M**
- **6 chains interconnecting a total 108 vias in the ceramic**

Table III.3

These 1-sided test structures with thin film conductors were successfully fabricated. After fabrication, these test structures were subjected to thermal cycle (-40°C to + 125°C) testing and did not exhibit significant degradation.

2-sided High Density Test Structures with thin film BCB polymer overlays

The test structures schematically shown in Figure III.1 were fabricated using the general test pattern shown in Figures III.2. However, the top layer (layer #1) conductor pattern was replaced with a 2 layer thin film conductor daisy chain pattern. This 2-sided pattern consists of 5 layers on the top side of the metal core (2 sacrificial layers for polishing) and 3 layers on the bottom side. The thin film pattern is deposited on the top side after polishing. The design of the conductors (both layers shown together) is shown in Figure III.4. The details of this design are shown in Table III.4.

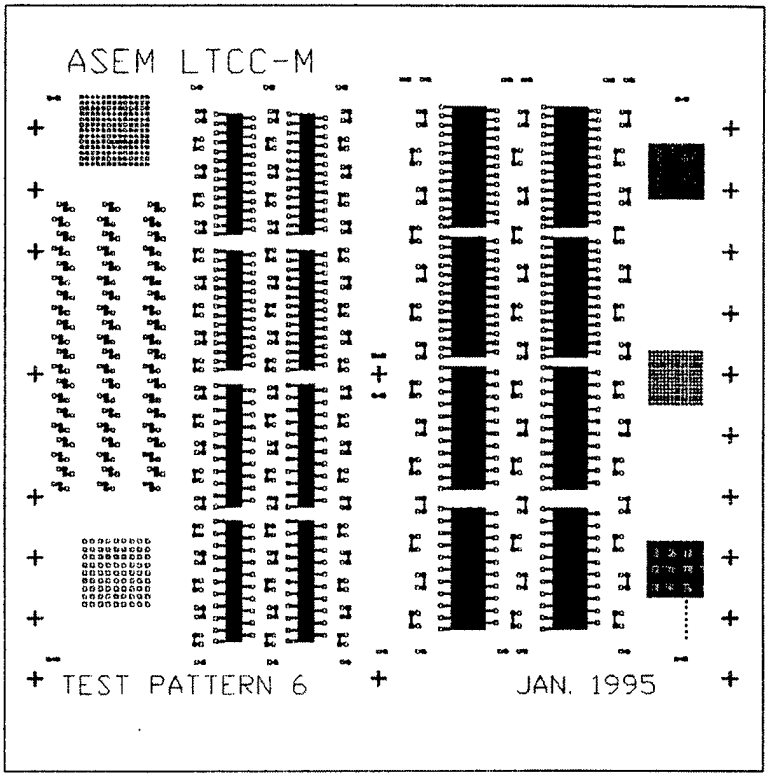


Figure III.4: High density thin film test pattern for LTCC-M

Layout Statistics 2-sided LTCC-M with BCB Overlay
•2 level BCB daisy chain
1 and 2 mil lines, spaces, and vias
3 mil diameter capture vias to ceramic vias
987 vias
16 meander line patterns
•8 layers of LTCC-M (total)
•Cu/Mo/Cu has 204 13 mil diameter electrical feedthroughs
•6 daisy chains interconnecting a total 1242 vias in the ceramic

Table III.4

High Density LTCC-M Test Structure

A high density test structure was also designed and tested. This structure is similar to the one described in Figure III.2 and Table III.1, except that the 8 mil diameter vias are reduced to 4 mil diameter vias and the 8 mil lines and spaces are reduced to 4 or 5 mil lines and spaces. The number of daisy chains and the number of vias connected within each chain are unchanged from Table III.1.

B. SILVER MIGRATION TESTING

The silver migration test pattern consisted of a parallel plate capacitor structure having 1 layer of green tape ceramic as the dielectric, a thick film silver buried electrode, and a thick film AgPd (30% Pd) top electrode. The test is performed in a temperature humidity chamber set for a constant temperature and humidity of 85°C and 85%RH. The voltage across the capacitor structure is 48 volts, with the top electrode negative relative to the buried electrode. Tests were run on 1-sided ABT-36 samples (4 layer samples) with the silver migration capacitors formed around the top ceramic layer.

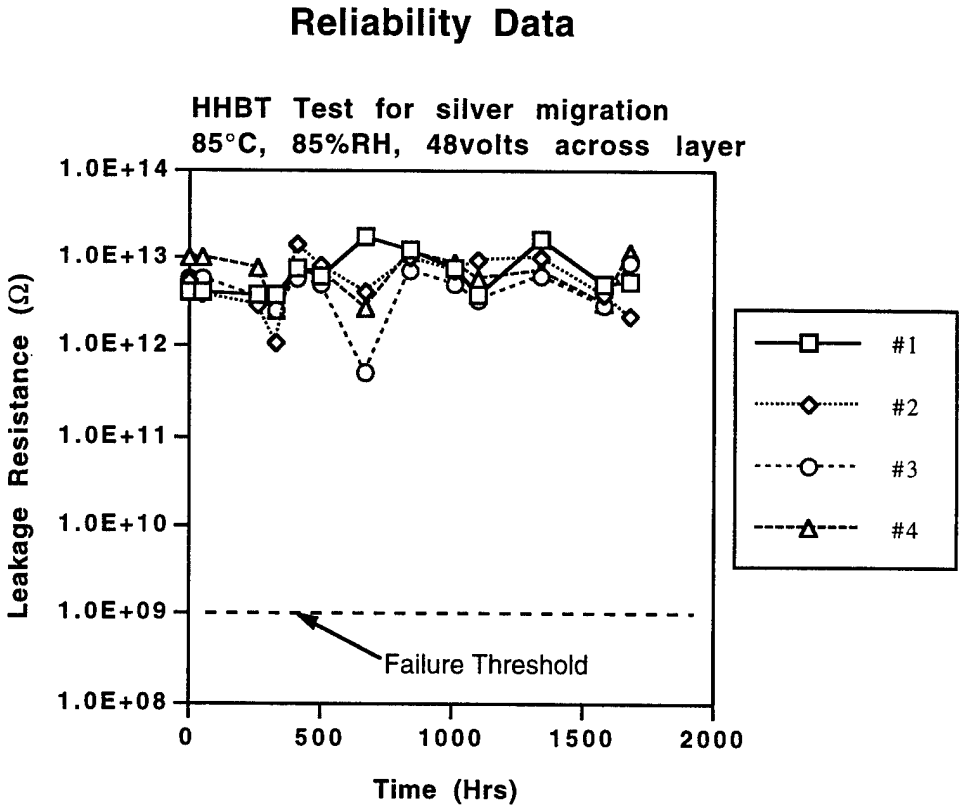


Figure III.5: HHBT test results show that the low porosity of the LTCC-M glass/ceramic prevents silver migration.

As can be in Figure III.5, silver migration **failures were not observed** in the ABT-36 ceramic. This verified that this ceramic sinters to a very high density during firing, which will prevent reliability problems due to silver migration.

C. THERMAL CYCLING AND HIGH TEMPERATURE STORAGE TESTS

The thermal cycle employed in all of the tests described in this report is between -40°C and +125°C, with a 30 minute dwell at each temperature. The temperature ramped up to 125°C in 1 hour, and ramped down to -40°C in 2 hours.

1-sided Test Structures

The results of the thermal cycling tests on 1-sided high density test structures are shown in Figure III.6.

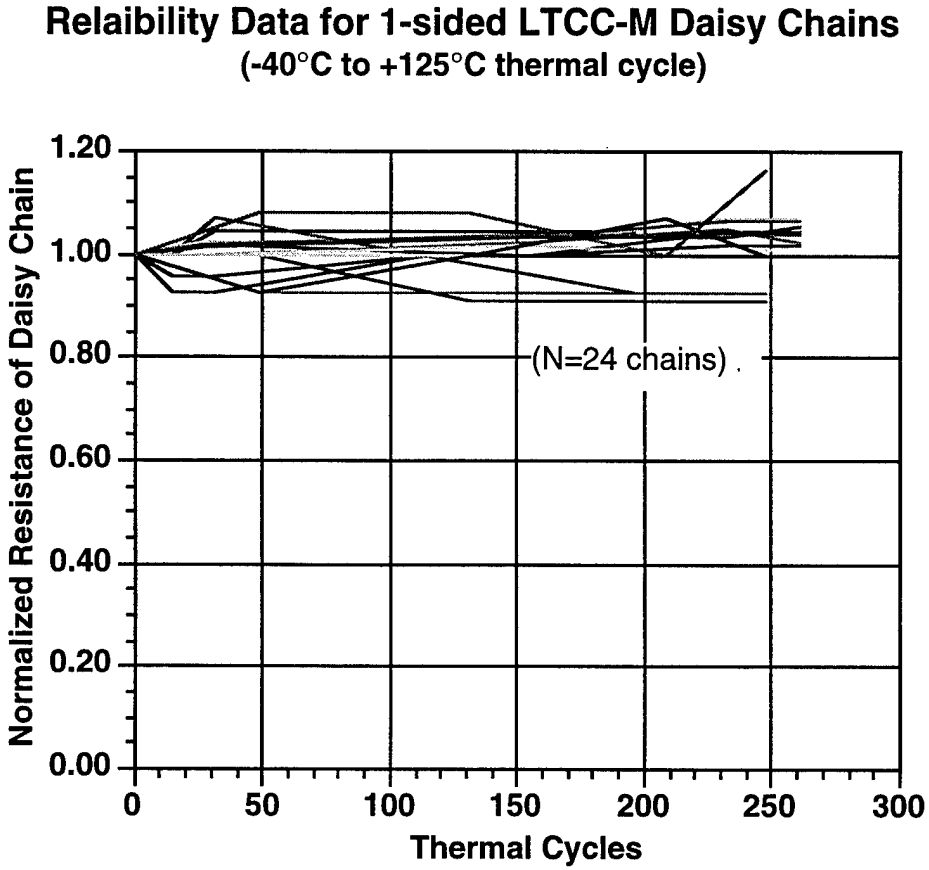


Figure III.6: Thermal Cycling results for 1-sided high density test pattern samples show no degradation.

Figure III.6 **shows that the resistance of each daisy chain remained constant** throughout the test period. Additionally, observation using a low power microscope (40X) did not reveal any cracking caused by the thermal cycle stresses. This indicates very good compatibility between the LTCC-M ceramic and the thick film vias.

2-sided Test Structures

The results of thermal cycling of 2-sided test structures (without thin film overlays) is shown in Figure III.7.

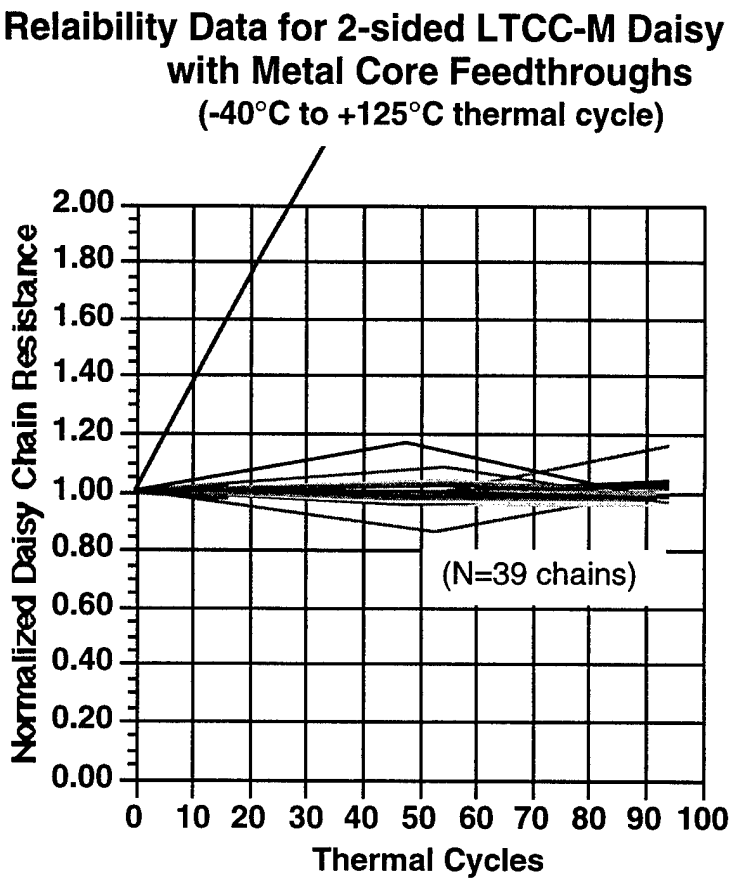


Figure III.7: Thermal Cycling results for 2-sided high density test pattern samples show no degradation.

Figure III.7 shows that **the resistance of the daisy chains for 2-sided LTCC-M samples having electrical feedthroughs remained constant**. Of the thousands of vias and feedthroughs tested, only one daisy chain link ever failed during thermal cycling. The fact that it failed very shortly after testing began, suggests that this was a marginal connection, and is not indicative the robust vias and feedthroughs that are produced by the LTCC-M process. Additionally, examination of the circuit boards with a low power microscope did not reveal any cracking of the vias. These results point to the good compatibility among all of the LTCC-M components.

Low Density Test Structures with thin film BCB polymer overlays

Sixty (60) thin film daisy chains (4 vias/chain) in BCB overlays on LTCC-M ceramic were subjected to 100 thermal cycles. The adhesion of the BCB polymer to the polished ceramic remained acceptable (it could not be removed by the scotch tape test) after 100 thermal cycles. Only 3 chains exhibited failure during this time. These failures started to appear early in the test (<24 cycles). Since all of these failures occurred in the same area of a single test sample, these failures were initially attributed to incomplete opening up of the via in the BCB dielectric by the plasma etch step. The fact that the vast majority (95%) of the daisy chains tested showed a constant resistance, indicated good compatibility between the LTCC-M ceramic and BCB polymer overlays.

An additional group of samples (150 daisy chains) having longer thin film daisy chains (8 or 15 vias/chain) were tested through 24-42 cycles. Their results also showed a constant daisy chain resistance, and are in complete agreement with samples that were cycled 100 times.

High Density Test Board Reliability Studies

Sets of high density test boards (4-layer boards with 9 daisy chains interconnecting a total of 978 vias; 4 mil diameter vias and 4-5 mil wide lines) were fabricated using green tape punched with 4 mil diameter holes and with the following materials: ABT-60 green tape; INJ-202B via ink; KMB-21D buried conductor ink and TC-9 top conductor ink. The high density via hole patterns were injection filled. The buried conductor ink used here was comprised solely of Ag powder Q and resulted in improved printability of the fine line traces relative to the mixed Ag flake/Q powder inks used previously.

Five parts from this group were subjected to temperature cycling (-55 to +125°C, 30 min. holds at temperature) and five parts were subjected to 150°C temperature aging; the resistances of the daisy chains were monitored as a function of test cycles or hours. A summary of the test parts and total test cycles or hours that each part underwent is given in Table III.5. **No significant variations in chain resistance were observed** in parts tested for about 600 temperature cycles and aged for up to 1800 hours at 150°C. Typical results for temperature cycling and temperature aging tests are shown graphically in Figures III.8 and III.9. In the this test pattern, chain numbers 1-3 are high density chains (4 mil diameter vias on 16 mil centers with one 4 mil wide line between vias; 120 vias per chain); chain numbers 4-6 are medium density chains (4 mil diameter vias on 30 mil centers with two 5 mil wide lines with 5 mil spaces between vias; 120 vias per chain); and chain numbers 7-9 are low density chains (4 mil diameter vias on 42 mil centers with three 5 mil wide lines with 5 mil spaces between vias; 84 vias/chain).

Table III.5: **Reliability Test Part Summary**

Part ID	Test	Total Test Cycles (-55 to +125°C)	Total Test Hours (150°C)
C1	Temp. Cycling	626	
C5	Temp. Cycling	626	
C6	Temp. Cycling	570	
D1	Temp. Cycling	595	
D3	Temp. Cycling	565	
C3	150°C Temp. Aging		1818
C4	150°C Temp. Aging		1818
C2	150°C Temp. Aging		1818
D2	150°C Temp. Aging		1727
D4	150°C Temp. Aging		1651

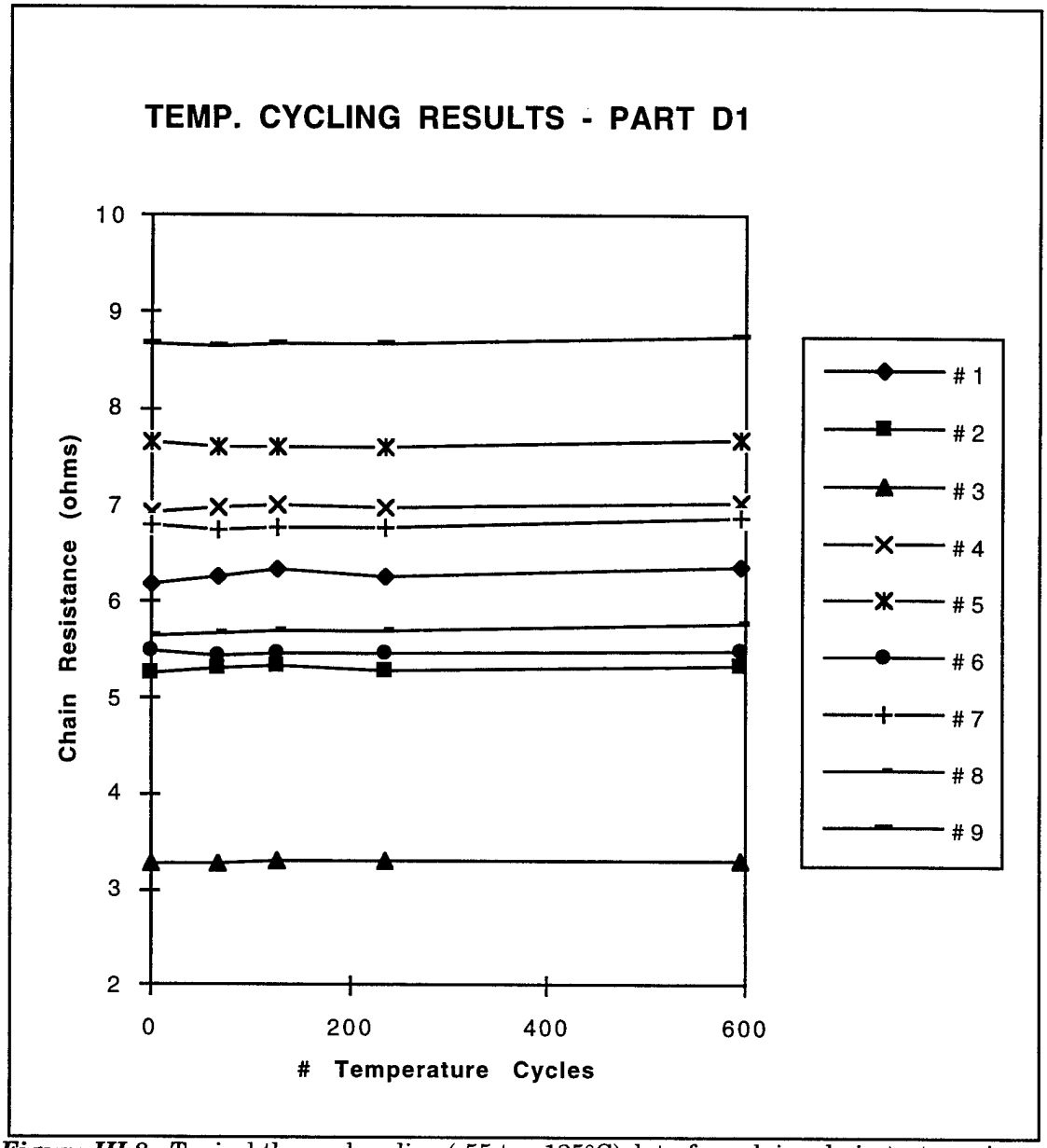


Figure III.8: Typical thermal cycling (-55 to +125°C) data for a daisy chain test specimen.

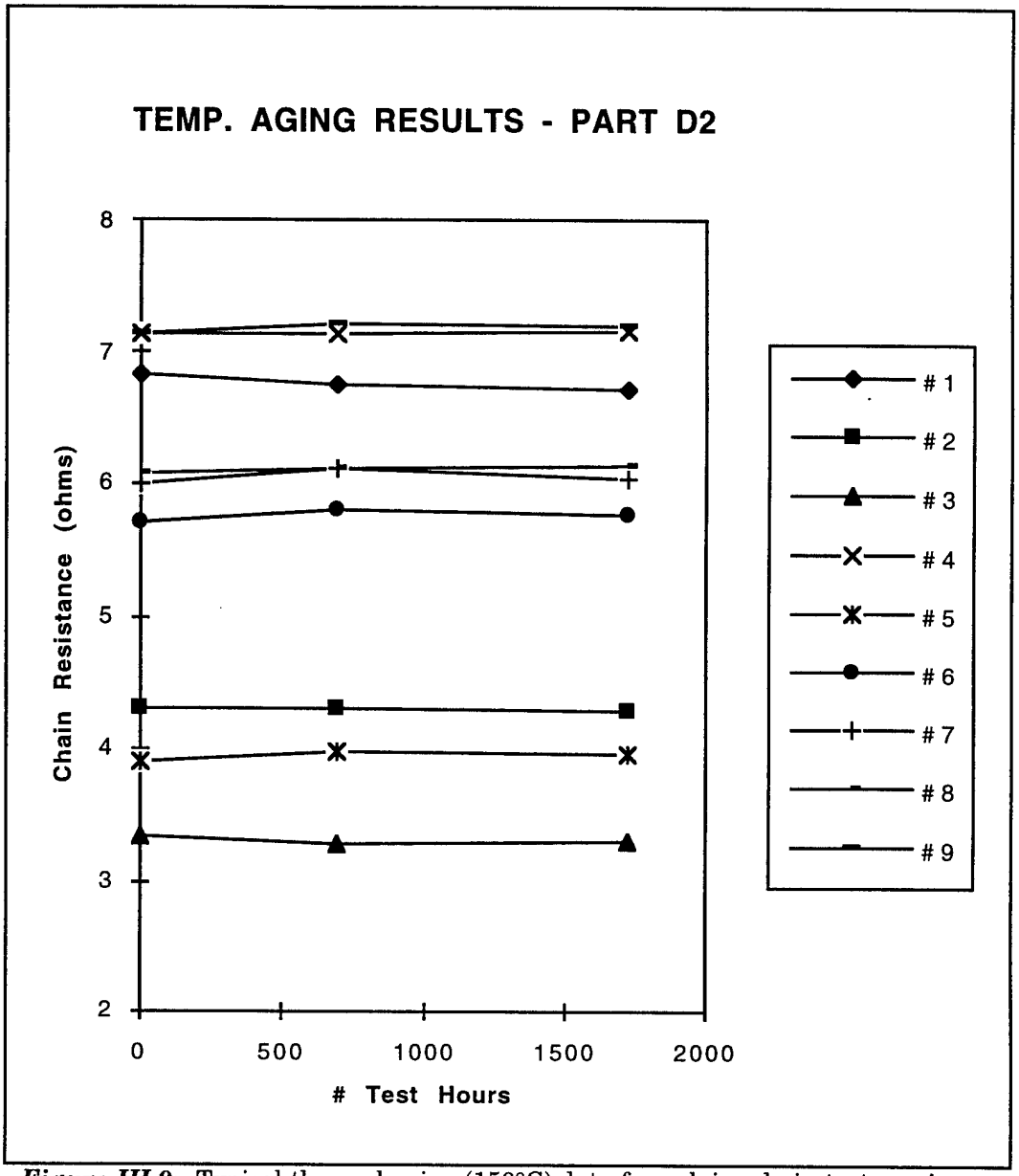


Figure III.9: Typical thermal aging (150°C) data for a daisy chain test specimen.

Ceramic to Metal Adhesion

The adhesion of the ABT-36 ceramic to the Cu/Mo/Cu metal core was measured by a pull test on an Instron Universal Testing Machine. Precut 7 m m squares of ABT-36 (4 layers thick) were colaminated onto a Cu/Mo/Cu core that was prepared for bonding. Prior to conducting the pull test, samples were subjected to thermal cycling from -40°C to + 125°C. As shown in Figure III.10, the adhesion of the LTCC-M ceramic to the Cu/Mo/Cu metal core was not significantly affected by 300 temperature cycles. This is a further indication of the excellent compatibility between the bonding process, the LTCC-M ceramic, and the metal core.

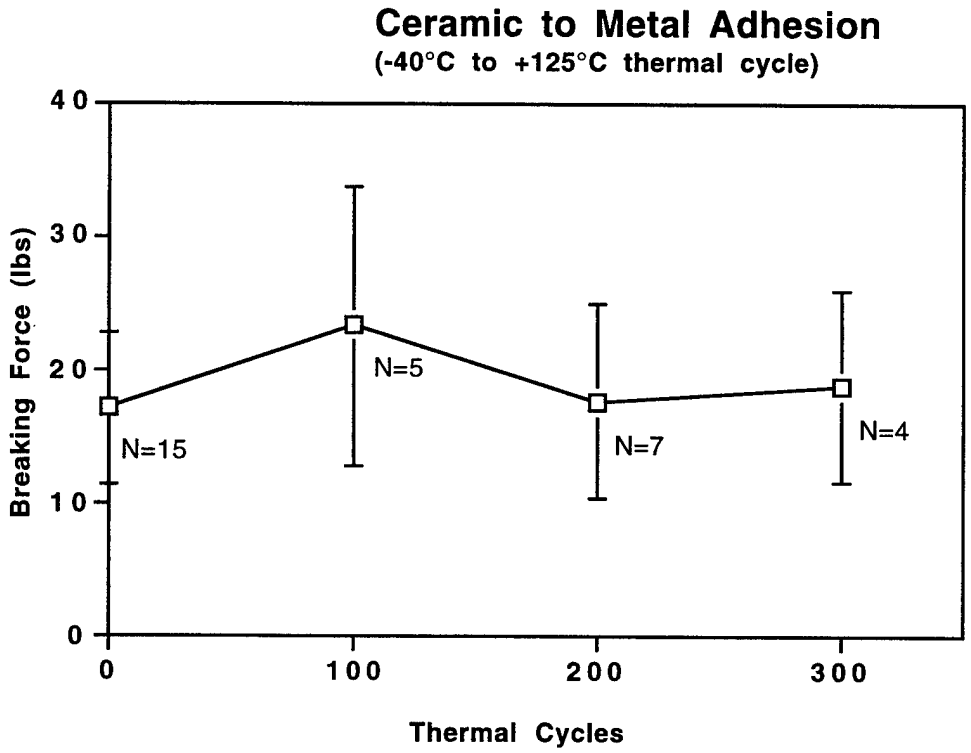


Figure III.10: Thermal cycling does not produce any significant change in the adhesion of the LTCC-M ceramic to the metal core.

Section IV
LTCC-M Technology Transfer to Dielectric Laboratories Inc.

A. INTRODUCTION

This section describes the Technology Transfer from the technology developer, Sarnoff Corp. to a merchant supplier, Dielectric Laboratories. The goal of this transfer was to duplicate all Sarnoff processing at DLI. This would position DLI to be able to scale-up the processing, as required. Since time was short, DLI opted to have several major processes performed by outside suppliers, including green tape casting and thick film ink making. The processing was slightly modified to accept these incoming materials, and produce substrates having nearly the same final properties as ones fabricated entirely at Sarnoff. The Technology Transfer was successfully completed in about 9 months, in a very interactive manner. Materials and samples were exchanged on a regular basis. Monthly meetings were held to review all progress, and to solve any recent issues as they arose. The principal goals and metrics for the LTCC-M Technology Transfer to DLI were as follows:

1. Duplicate the processes that have been set-up within Sarnoff at DLI
2. Process baselines to be established by exchange samples of all major processes and materials for measurement and additional processing at both locations
3. Validate the technology transfer by production of test structures demonstrating all primary LTCC-M process steps
4. Fabricate 20 C-band power amplifier packages, to design built by Sarnoff, for evaluation by Raytheon

During this interactive Technology Transfer a large number of technology issues were observed and solved. Many of these problems are listed in Figure IV.1.

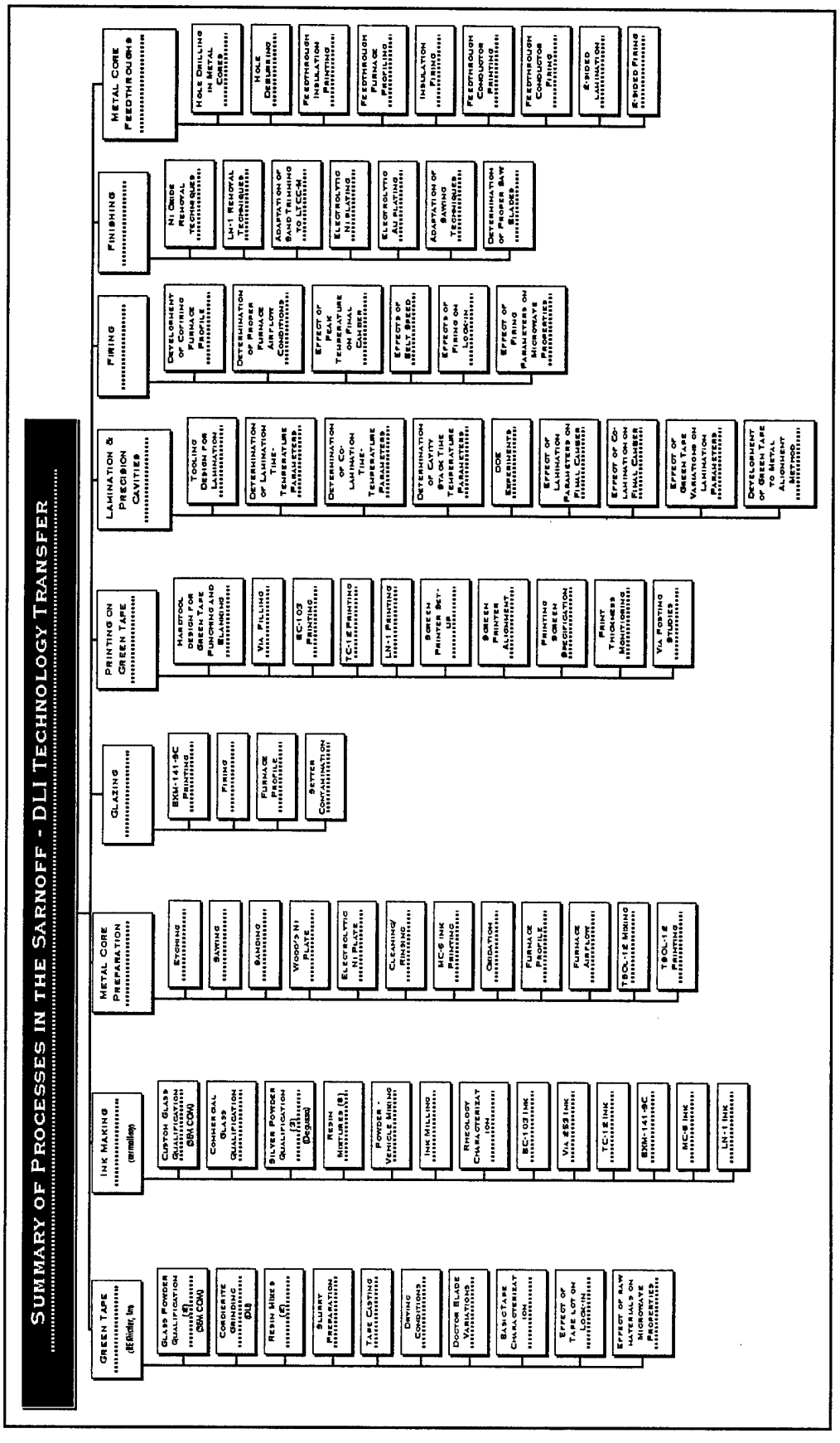


Figure IV.1: List of the processes and issues addressed during the Technology Transfer to DLI.

B. TECHNOLOGY TRANSFER TO DIELECTRIC LABORATORIES INC.

General

Technology Transfer Training

Technology training sessions were held at Sarnoff Corporation with DLI personnel receiving instructions, detailed handouts and hands-on training with Sarnoff equipment and materials. These training sessions covered all areas of the LTCC-M technology required for fabrication of the C-band Power Amplifier Technology Demonstration Module.

Materials, Processes and Equipment

During the year DLI established a relationship with all of the vendors supplying raw materials, purchased a supply of materials and qualified them for use. These included Sem-Com for glass, Degussa for metal powders, Heraeus Cermalloy for thick film inks, Richard E. Mistler for tape, and CSM for metal cores. All tooling required to complete the technology transfer was also purchased. Critical equipment necessary to complete the goals of this project, such as a furnace, screen printing machine, lamination presses and computer controlled saw for singulating parts were all purchased. Finally, a plating line was set up and qualified.

Green Tape Casting

A total of nine production lots of tape, varying from 50 to 80 feet long and 6.75 inches wide have been received from Richard E. Mistler and evaluated. Electrically, the various lots have all had acceptable dielectric constant (~5.6) and Q values (700 - 1000) when measured, between 12 and 13 GHz, at DLI. All lots have had acceptable lock-in when tested using a 6 layer, 2.5 inch square stack of tape laminated and fired on a metal core. Early in the qualification process DLI found that they were not getting the same camber values that Sarnoff got with their tape. The tape formula was adjusted to compensate for this camber difference.

Problems have been encountered in purchasing tape with consistent and uniform thickness. Tape thickness has ranged from 0.007" to 0.010" from lot to lot. Another problem is that tape thickness across a the width has varied as much as +/- 10%, being thicker in the center. Tape has been manufactured using multiple lots of glass purchased from Sem-Com, with good results. In addition DLI has demonstrated that tape made with cordierite, milled at DLI using standard ball milling procedures, produces acceptable tape

The continuing problem of getting consistent results from lot-to-lot has made it difficult to pinpoint the cause of problem areas such as lock-in and adhesion variation, singulation cracks, and camber variations. DLI can not specifically attribute problems to tape variances, but until they get consistency they can not eliminate it as contributing to the problems just mentioned.

Metal Core Preparation

Much of the effort to transfer technology to DLI was used in understanding issues related to metal core preparation and actual processing of the core. This was time well spent since this is critical to the successful fabrication of actual parts. This work cell covers core machining, core preparation for Ni plating, the actual plating process, and oxidation of the core with and without metal contact conductor, MC6. During the technology transfer DLI developed one outside

source to EDM unusual shapes and features into the metal core for manufacturing the C-band amplifier deliverable and another source to drill holes through the core for demonstrating two-sided manufacturing capability. DLI also developed an internal capability to deburr parts after any sawing or machining process.

During the year DLI spent a great deal of time on plating and plating related processing. At times during the learning curve they had problems related to both the plating materials and the plating process. They discovered that initial "poor plating (a black surface color)" was due to a contaminated Wood's nickel strike bath. After changing the bath, the plating became silvery and bright metallic as expected. DLI also saw differences in the visual appearances of parts plated at Sarnoff and those plated at DLI. These were believed to be causing problems later in the process. It was discovered that this visual difference was due to small learning curve variances. As more experience was gathered and understanding of the process improved, the differences became less significant. DLI also observed visual anomalies in plated parts after oxidation. These were yellow discolorations and glassy specks in the oxide layer that were not seen in parts oxidized at Sarnoff. Over time it was determined that cleanliness is the most important factor in minimizing these last two defects. During the year DLI also demonstrated the capability to plate multiple cores at the same time and cores up to 6" X 6.

At this time DLI understands the plating process and material control requirements necessary for plating and typically have good results The oxide fires with a dark green color and adhesion of the oxide to the core is good. Occasionally, there are still occurrences of yellow discoloration and glassy specks, and DLI continues to try and determine the cause of this.

Thick Film Ink Formulation and Printing Cell

As with the green tape, DLI chose to have inks manufactured by an outside vendor because of time constraints with the program. The manufacturer chosen was Heraeus Cermalloy. Initial lots of materials were made to Sarnoff specifications using silver powders and Sem-Com glasses ordered by DLI and shipped to Heraeus. The first lots of conductor and glass inks had some visual differences from Sarnoff prepared materials. These were not deemed to be significant. A greater problem was that there were viscosity variations that resulted in slight process differences from Sarnoff materials. Despite these differences DLI was able to make product successfully. Over time changes were made at Heraeus to correct both the visual and the viscosity discrepancies compared to Sarnoff prepared materials.

Of all the materials the greatest difference is with the Vias 253 ink. The rheologies of the materials prepared at Sarnoff and Heraeus are very different. Sarnoff material has the consistency of dream whip while Heraeus material flows very well. The Heraeus material, as a result is more forgiving and vias fill very well. The remaining issue is that DLI gets more posting with the Heraeus material then the Sarnoff material. This may be due to solid loading differences with inks and/or tape shrinkage differences from Sarnoff tape. This is still a critical area that needs to be addressed for actual production manufacturing.

Top conductor, TC12 prints well and is acceptable for line widths and spaces 0.008" and higher. One problem is that the ink has a tendency to dry

quickly in the screen, limiting throughput. DLI has been evaluating new Sarnoff inks with a slow drying vehicle. This change has improved the manufacturability of the material. Additional work still needs to be done and we are going to evaluate a fine print ink using silver powder in place of silver flake. Adhesion of the TC12 is still and issue. Work to date indicates that this is thickness dependent. A minimum dried TC12 thickness 20 microns is our target to insure adequate adhesion.

In general, the inks from Heraeus Cermalloy work well with the DLI process, and where adjustments were needed Cermalloy was helpful in working to improve the materials. In addition, DLI personnel have quickly gained the expertise necessary to print parts with more complexity than is typical of DLI standard products. As a result, minimal issues have occurred with screen printing prototype quantities of parts.

Lamination and Precision Cavity Processing

The lamination process was established to match the Sarnoff process as close as possible. DLI used the same tooling designs, tooling materials and lamination parameters as Sarnoff. Even so they had some problems early in the implementation stage. It was discovered that Sarnoff and DLI presses were not laminating at the same pressure for a given gauge reading. DLI was actually laminating parts at a higher force, resulting in parts that were bowed more then expected and had poorer lock-in. Once this discrepancy was eliminated lamination differences became negligible. This helped DLI to understand how excess lamination pressure can cause problems after cofiring and gave them a greater understanding how this can effect their results.

Another problem occurred when laminating parts with cavities. DLI had significantly more rounded corners on cavities then Sarnoff processed parts. Again DLI discovered that they were not using the same process as Sarnoff. When the procedure was changed the edge rounding decreased significantly.

At this time DLI does not believe that they have any problems related to lamination, although they do believe that there is more that needs to be understood to help improve the process. To accomplish this DLI started a lamination matrix to evaluate the process. So far they have determined that it is not necessary to rotate tape in order to get consistent lamination. Additional work will be done in this area.

Firing

As with other processes, DLI tried to match firing profiles in their furnace as close as possible to the Sarnoff profiles. The camber of parts fired in the DLI furnace did not match that of parts fired in the Sarnoff furnace. In addition, the electrical properties of the fired dielectric were not very good; Q values, were low. DLI determined that the thermocouple used to profile the furnace was not calibrated, and actual temperatures were 30° below the target temperatures. This temperature difference was masked by the fact that the furnace settings also indicated that the furnace was at the right temperature. This was the cause of both the camber variation and low electrical properties. When DLI changed the thermocouple and adjusted the profile, the problems corrected themselves.

During early transfer efforts DLI was also having problems getting oxidized parts to look similar to Sarnoff oxidized cores. Typically DLI parts were

more greenish with yellow streaks. It was determined that part of the problem was low air flow in the furnace. DLI spent a great deal of time trying to increase the air flow to match Sarnoff and was successful in matching the overall flow numbers. They also noted visual differences when using metal contact (MC6) to electrically connect to the core. The MC6 contains boron to reduce the nickel oxide and the fired part has a "color plume". The DLI "plume" never looks the same as the Sarnoff "plume", but electrically no difference can be seen. Once the MC6 was shown to fire good, a number of 36 hole test parts, with up to three layers of filled, stacked vias, were fabricated. After firing, the electrical continuity of all vias to the metal core were verified, demonstrating that we were making good contact from the MC6 through the oxide to the metal core.

Once the profiles were established DLI results were good. The glasses fired as they should and were visually similar to Sarnoff parts. The cofiring profile resulted in good electrical values and lock-in of the tape to the core. Finally, oxidation/firing produced parts that produced acceptable results.

Top Conductor Plating Cell

DLI successfully demonstrated that they can, electrolytically plate the top conductor in a finished LTCC-M part. The Sarnoff 36 hole test was used for this purpose. The initial plated parts showed attack of some metal pads as a result of the plating process. Additional efforts have optimized the process and the results today are good. DLI has also demonstrated that they can electrolessly Ni/Au plate using the new plating system recommended by Sarnoff. In addition, as part of this work cell, they have developed a new process for removing LN1 from any exposed surface and for stripping oxide from the cavity areas and any areas of exposed metal. This process utilizes a standard DLI technique, sand abrasion. DLI has optimized the process so that they can remove both LN1 and oxide simultaneously without damaging top conductor or core, in a cost effective manner.

Singulation

During the build of C-band deliverables DLI discovered that there were problems related to singulating individual parts from the multi-up core using a K&S automatic sawing machine. DLI originally tried to simulate the Sarnoff process but was not successful in this. When parts were inspected after sawing, cracks radiating from the core to the ceramic surface were discovered. DLI also found cracks that propagated under the cavity side wall onto the top of the part. A major investigation was started to solve this problem. This included internal efforts with DLI engineers to optimize the sawing parameters and with engineers from Thermocarbon and K&S to look at both the blade and the machine parameters. DLI discovered that any part that needed to be electrolytically plate had to be cut through both the fired ceramic and metal core at the same time. Typically, sawing these two dissimilar materials requires two totally different blade materials and sawing parameters. Over time DLI was able to eliminate the cracking through the use of optimized blade materials and configurations.

During the time DLI optimized the sawing process they also investigated a process to cut streets, between adjacent parts, in unfired tape already laminated to the core. The concept was a modification of the Sarnoff robot process. The objective was to remove the material in the streets before firing so that only the

metal needed to be sawed. The DLI process utilized a printed wiring board router to remove the tape rather then the two parallel blades in the Sarnoff process. The original demonstration worked well and this process looks very promising.

Metal Core Feedthrough Cell

The technology transfer related to this area was successfully completed. As discussed above, a local printed wiring board manufacturer was identified and supplied us metal cores with holes drilled in them using the 36 hole test pattern. The holes were inspected and visually are acceptable. The holes were then deburred, plated and oxidized with good results. DLI sent the two-sided deliverables to Sarnoff where they were temperature cycled from -40°C to +125°C. After 101 cycles the parts were still good. Both parts showed continuity through all feedthroughs, and maintained greater than 20 M_ isolation from the Cu/Mo/Cu core.

Deliverables

All deliverable items were manufactured at DLI and sent to Sarnoff in completion of the program requirements. They included the following:
Two tape lots from Mistler
Plated Cu/Mo/Cu Core Samples
LTCC-M Fired Samples
Ground Via Contact Samples
Top Metal Plated Samples
Two samples of LTCC-M with Feedthroughs (two-sided test modules)
C-Band Power Amplifiers

Summary

The original transfer of technology from Sarnoff to DLI, using training sessions at both facilities, was completed with good success. This mutual effort was continued through the course of the program and was a major reason why this effort was successful. The ability to use Sarnoff as a resource to assist in problem solving was instrumental in shortening the cycle times needed in these efforts.

Tape made by Mistler and thick film inks made by Heraeus appear to be acceptable but additional work needs to be done to optimize them. All metal core processing processes, such as machining, throughhole forming and core plating are working well. After a great amount of effort in the area of plating, DLI now believes that plating is no longer an issue.. Printing of all materials has quickly learned and has not been an issue during the transfer of this technology. Lamination was identified as a possible cause of camber on fired cores and this was verified through a test matrix at DLI and Sarnoff. The lamination process has been qualified and is well controlled. Samples with cavities have been made and no problems were seen. Firing was initially a problem, however, all profiles have been adjusted and firing is acceptable. Top conductor on test parts were successfully plated, both electrolytically and electrolessly, and these are acceptable. DLI has established both electrolytic and electroless plating lines. A manufacturable process to remove LN1 from the exposed tape surfaces and Ni oxide from all metal surfaces has been developed beyond the requirements of this program. Singulation is still an issue, especially for high volume

manufacturing, that will require additional development. All deliverables required by the program were completed and accepted by Sarnoff.

Section V
Technology Demonstration Vehicles

A. INTRODUCTION

The four technology demonstration vehicles planned for this program were chosen because each module had clear military applicability, and also met the requirements of the consumer marketplace. These modules were: (1) an optoelectronic transceiver module, (2) a power amplifier package, (3) an advanced PCMCIA card, and (4) a Power Electronic Building Block (PEBB). Table V.1 shows the application of each demonstration module to the needs of the US armed forces.

Table V.1:
Military Relevance of LTCC-M Technology Demonstration Vehicles

Prototype Application	Supporting Co.	Type	Military Relevance
Advanced PCMCIA Card (ORBCOMM Modem)	Torrey Science	Mixed Signal Module	1. Similar electronics needed for global tracking of high value and critical military materials and components (e.g. armaments) 2. Supports DoD: • Materials Command • Logistics Command • Transportation Command • "Total Asset Visibility" program 3. Technology applicable to the following: • NSA (R2) dual function PCMCIA card • Trackers • Message Terminals • CESEL • Special Forces replacement of high frequency radio systems (miniaturization) • Global extension of communications in Force 21 "Digital Battlefield" 4. Applies to Military Global Mobile Information Systems
High Power Motor Controller (Power Electronics Building Blocks)	Harris	High Power Single Chip Package	1. Supports US Navy Contract # N-00024-94-C-4088 (an Advanced Tech. Demo. with Naval Sea Systems Command) 2. Computer controlled Integrated Variable Speed Electric drive for ships (surface and subsurface) and tanks 3. Computer controlled Electric Actuators for airplanes, ships, and tanks 4. Auxilliary Power Unit Generators, Solid State Power Controllers for airplanes 5. Power Inverters and Converters for ships and airplanes
Optoelectronic Transceiver Module	AMP	MCM	1. Supports the construction of low cost broadband networks at military bases and installations. 2. Such networks support: • ATM based switching architectures • Transfer of large amounts of graphical and multimedia data • Digital signals • Encrypted signals 3. Supports ARPA contract "Manufacturable Low Cost Single-Mode Bi-directional Links for Fiber in the Loop Optical Networks" • Currently LTCC-M is the sole technology for this application
Power Amplifier Packages (microwave)	Raytheon	GaAs single chip package	1. Portable government cellular communications systems and wireless LANs 2. Applies to Military Global Mobile Information Systems

B. OPTOELECTRONIC TRANSCEIVER MODULE

Under this program Sarnoff, and AMP developed a package to integrate an optoelectronic MCM, an optical fiber, several silicon devices, and several passive components. This program provided tested bare-board LTCC-M packages to AMP for module assembly.

To meet the various design configurations of AMP, two similar packages were designed and fabricated together in a multi-up format. The decision to fabricate the "A" and "B" designs together minimized the overall NRE costs for building this package.

1. Challenges of this package

- Use of large area solid ground planes and shielding structures on all layers for noise immunity
- Crosstalk minimization
- Need for high precision cavities to minimize bond wire length of the high speed interconnections, especially the 1.2 GBit/sec link
- Need for a high thermal conductivity base for laser stability and thermal management
- Package must be hermetic

2. Package Description

Size: 0.54" x 1.10"

Components interconnected: Optoelectronic MCM, 2 bare ASICs (Si), resistors and capacitors

Interconnect density: general design with 8 mil lines/spaces and 8 mil diameter vias; 6 mil lines and spaces in the bond pad areas.

Number of layers: 3

Number of vias: 258

Number of component mounting cavities: 2

Number of nets: 26

3. Module Fabrication

In May, 1996 thirty (30) packages were delivered to AMP for module assembly and testing. **These packages were produced with a 90% bare board test yield**. These modules were designed for use with 2 mm square ASICs. However, the die that were delivered to AMP (under a separate DARPA program) were too large (and out of spec). Sarnoff has never been informed that AMP ever received properly sized die that will fit into the package cavities, nor has AMP delivered any package performance data from the packages delivered by Sarnoff.

The package designs, shown in Figure V.1(a) and (b), were approved by AMP. After conversion into an AutoCad file, hard tools were designed and screens were fabricated.

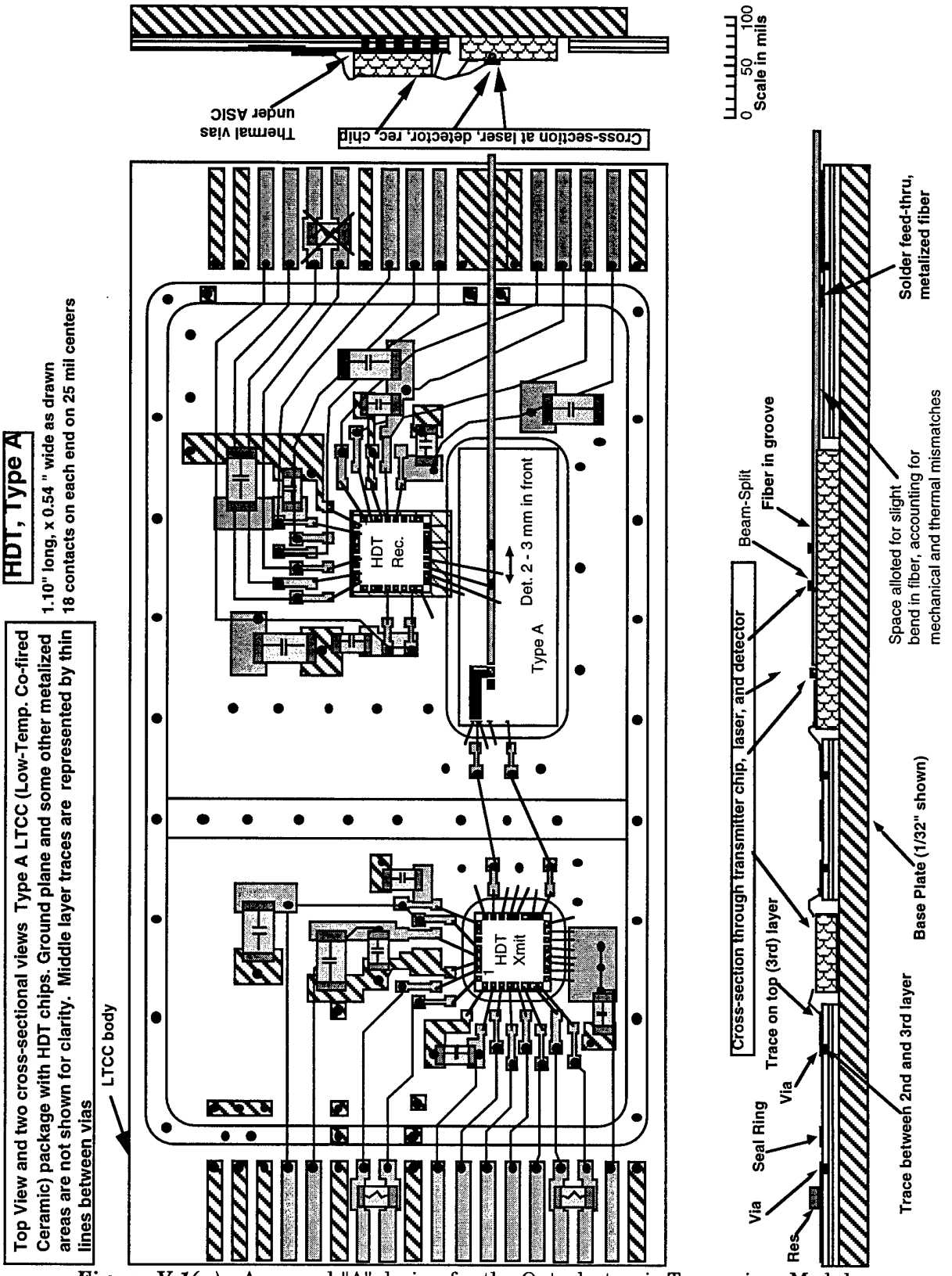


Figure V.1(a): Approved "A" design for the Optoelectronic Transceiver Module.

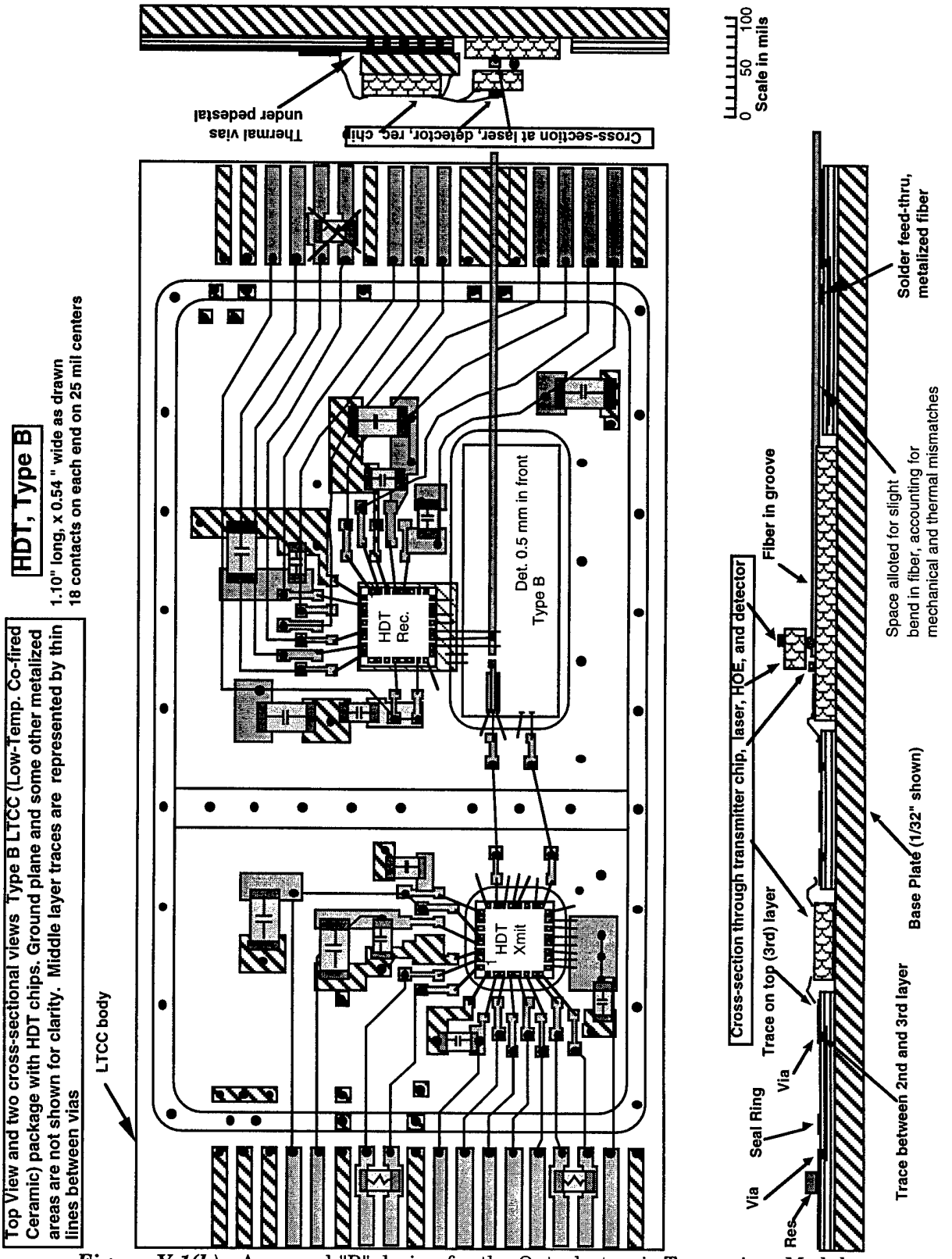


Figure V.1(b): Approved "B" design for the Optoelectronic Transceiver Module.

Based on the design furnished by AMP it was decided to build this package in a multi-up configuration (having both the "A" and "B" designs) using 3 layers of green tape stack that was attached to a 20 mil thick Cu/Mo/Cu base. All thermal vias contacted the metal base (not the glass bonding layer). The conductor pattern on the top layer of the package would plated by electroless Ni and Au plating baths. Finally, 63/37 eutectic Sn/Pb solder was printed and reflowed to the seal ring area.

This required the design of 3 stencils (1 for each via layer), 6 printing screens (4 conductors, 1 bonding layer, 1 LN-1 layer), and 1 cavity punch (for punching all cavities simultaneously). Green tape formulation ABT-52 SC was cast 8 mil thick for making these parts . After cutting into 3-1/4" squares it was sent to Schneider and Marquardt (Newton, NJ) for via punching. Vias for all layers were filled with thick film ink Via 253 using stencil filling techniques. All buried conductors were screen printed using thick film ink BC-103. The top conductor pattern was printed with ink TC-10, which after drying was overprinted with a fritless silver ink, BC-110. The use of a fritless silver overprint produced the best surface for wirebonding. To insure that the cavities maintained their "as punched" dimensions after firing, ink LN-1 was printed within the seal ring area, exposing only the bond pads.

After all screen printing was completed, the green tape layers were stacked using pin alignment fixtures and laminated. The lamination conditions were 3000 lbs and 185°F for 2 minutes. Next, the cavities were punched into the laminated green tape stack. Then the green stack was co-laminated onto the previously prepared Cu/Mo/Cu core. Co-lamination conditions were 600 lbs and 185°F for 2 minutes. The packages were then fired in a 9 zone Lindberg belt firing furnace (air atmosphere) with a peak firing temperature of 900°C.

After firing, the LN-1 material was removed by brushing with water. To smooth out the bonding pads, the top surface conductors were polished with a mildly abrasive slurry. At this point, the top surface conductors were plated by Pd activation, followed by a 5 - 10μm thick electroless Ni deposition, followed by a 8 - 10μin immersion Au deposition. The boards were then sent to Circuitest (Nashua, NH) for bare board testing (shorts and opens based on the netlist). Sixty circuits were tested, and the boards showed a first pass yield of 90%.

Solder (63/37 Sn/Pb) paste was then screen printed over the seal ring and reflowed on a temperature controlled hot plate (230°C). After flux removal, the circuits were diced into individual packages using a composite saw blade. Figure V.2 shows a tested package. Figure V.3 shows a package with a corner intentionally chipped away to expose the solid embedded ground planes, extending to within 5 mils of the package boundaries, required for electrical shielding. After final cleaning, the individual packages were shipped to AMP Inc., for module assembly and evaluation.

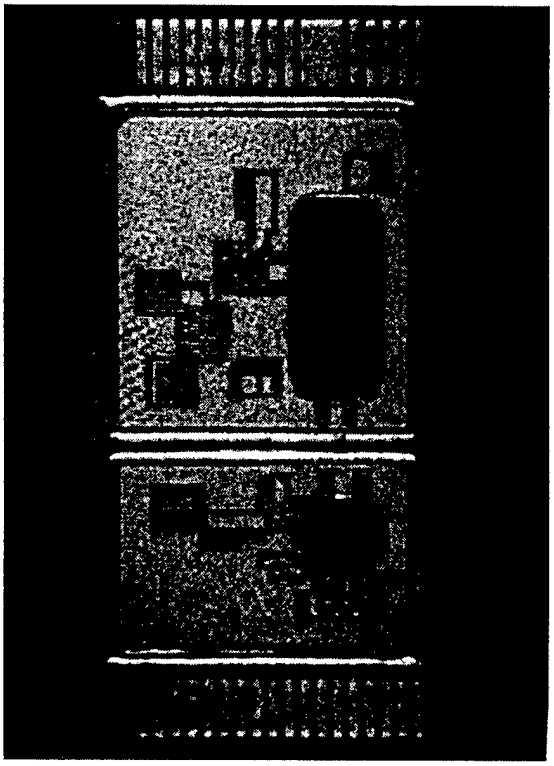


Figure V.2: An optical transceiver package (0.54" x 1.1") fabricated using LTCC-M substrate technology.

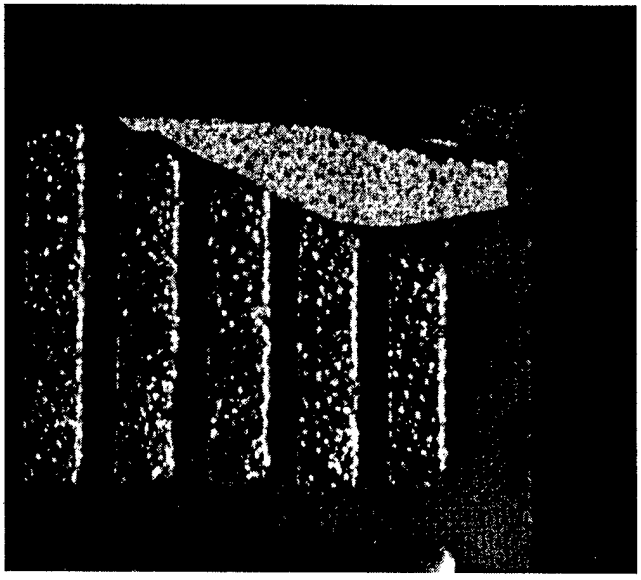


Figure V.3: An optical transceiver package with a corner intentionally chipped away exposing solid ground planes extending to within 5 mils of package boundaries.

4. Lessons Learned

The primary cause of yield loss during bare board testing was shorts from bond pad locations. It was noticed during screen printing that there was some ink smearing from the friless Ag overprint. This can be corrected by designing a separate screen for the overprint that only contains the bond pads, and not the shielding. The shielding does not require any overprint. This was not done during this first build because a "pads only" design was not supplied.

C. POWER AMPLIFIER PACKAGE

The objective of this task was to design, fabricate, assemble and test a low cost power amplifier package for a GaAs microwave device. The package was be designed, assembled and tested by Raytheon and fabricated by Sarnoff.

1. Challenges of this package

- Low loss microwave package for operation at C-band frequencies
- Integral metal base to minimize "moding" effects
- Need for high precision, tiered cavities to minimize bond wire lengths from die to package
- Need for a high thermal conductivity base for 10W power dissipation
- Thermal expansion match to GaAs for solder attachment of bare die to metal base
- Low loss transmission lines through seal rings

2. Package Assembly and Evaluation

As part of its evaluation of the suitability of LTCC-M to microwave packaging, Raytheon designed an LTCC-M package for its PA92 power amplifier. A demonstration LTCC-M package, shown in Figure V.4, was fabricated for use in a high output power (38 dBm) C-Band microwave amplifier. The amplifier has 27 dB of gain and is 45% efficient. Each package contained a bare GaAs die and 18 surface mount capacitors. Within an accurately sized cavity in the ceramic, The GaAs die was eutecticly soldered to the Cu/Mo/Cu metal base. The PA92 IC die consists of two electrically independent power amplifiers in a mirror imaged layout. The two amplifiers are connected together on chip in operation, and are matched to a 25Ω source and load impedance at the RF input and output ports. The PA92 meets the following requirements:

Parameter	Performance
Frequency	4.3 - 5.1 GHz
Output Power	≥ 38dBm
Gain	≥ 27dB
Efficiency	≥ 40%

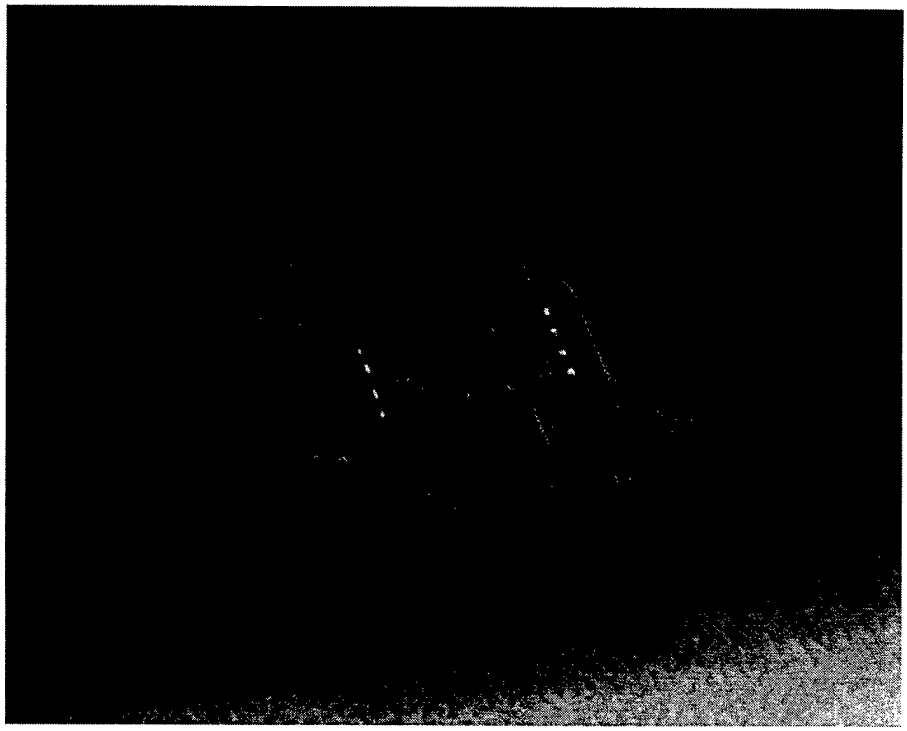


Figure V.4: 38 dBm C-Band power amplifier with integrated impedance transformers in an LTCC-M package.

In order to match the amplifier to 50Ω, a one stage quarter transformer was designed into the package at both the chip's input and output. In order to measure the insertion loss and return loss of the package itself, without the chip, two 50Ω lines were epoxied in parallel inside the chip cavity in place of the chip. Three wirebonds were connected to both sides of each 50Ω line. Typical insertion loss and return loss are shown in Figures V.5 and V.6 respectively. In the region of operational interest, between 4.1 and 5.3GHz, the return loss is less than -13.8 dB and the insertion loss is between -0.58 and -0.83dB. This data is good for a package of this size. The measured data includes effects of transmission lines epoxied inside the package cavity, the wirebonds, and the fixture connectors. The null in the package's insertion loss response between 3.9GHz and 5.5GHz is attributed to the inductance of the wirebonds.

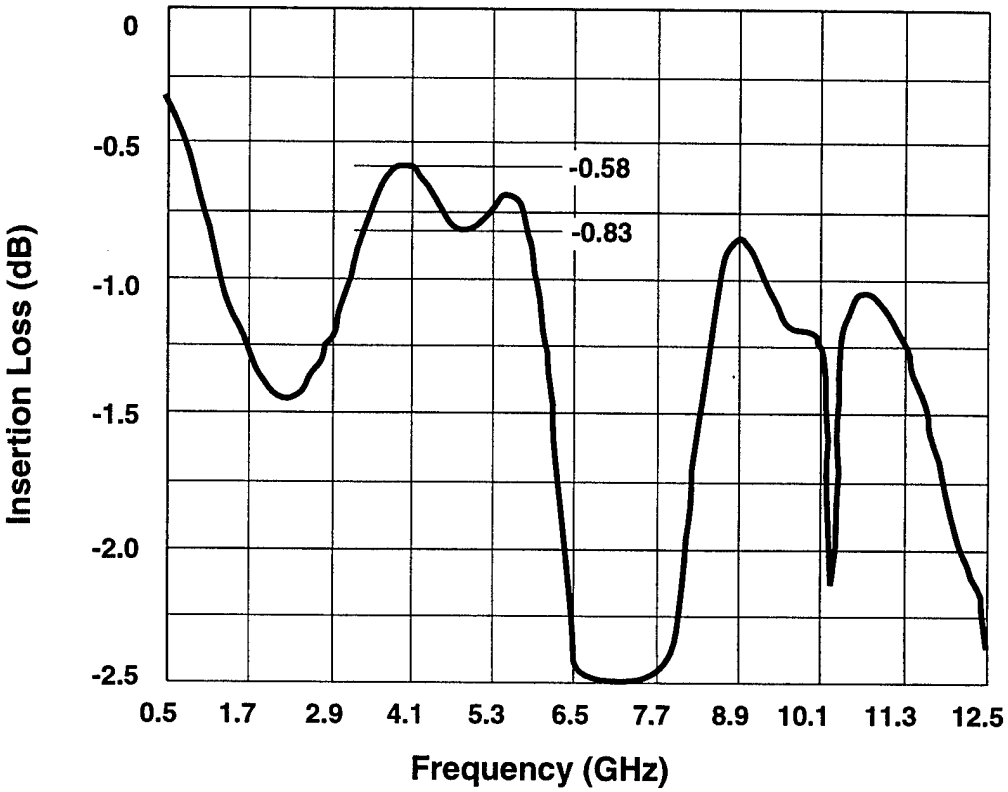


Figure V.5: Insertion loss response of the LTCC-M C-Band Package.

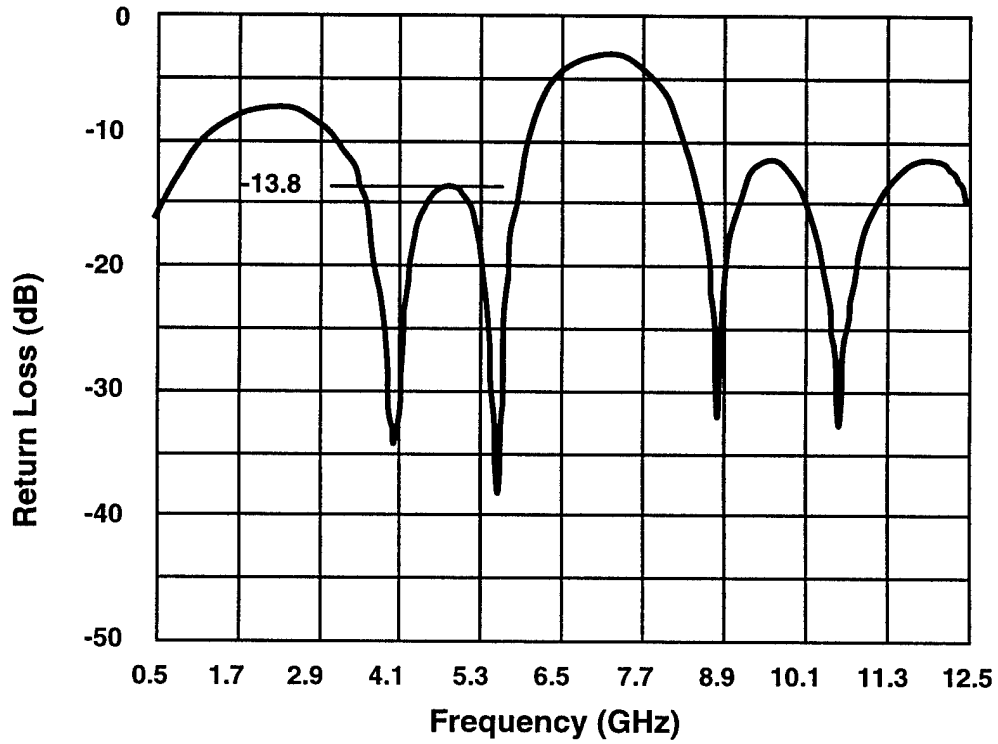


Figure V.6: Return loss response of the LTCC-M C-Band Package.

Figure V.7 shows the results of tests made on the fully assembled amplifier in the LTCC-M package. The package is capable of handling 38 dBm of output power at efficiencies greater than 45%.

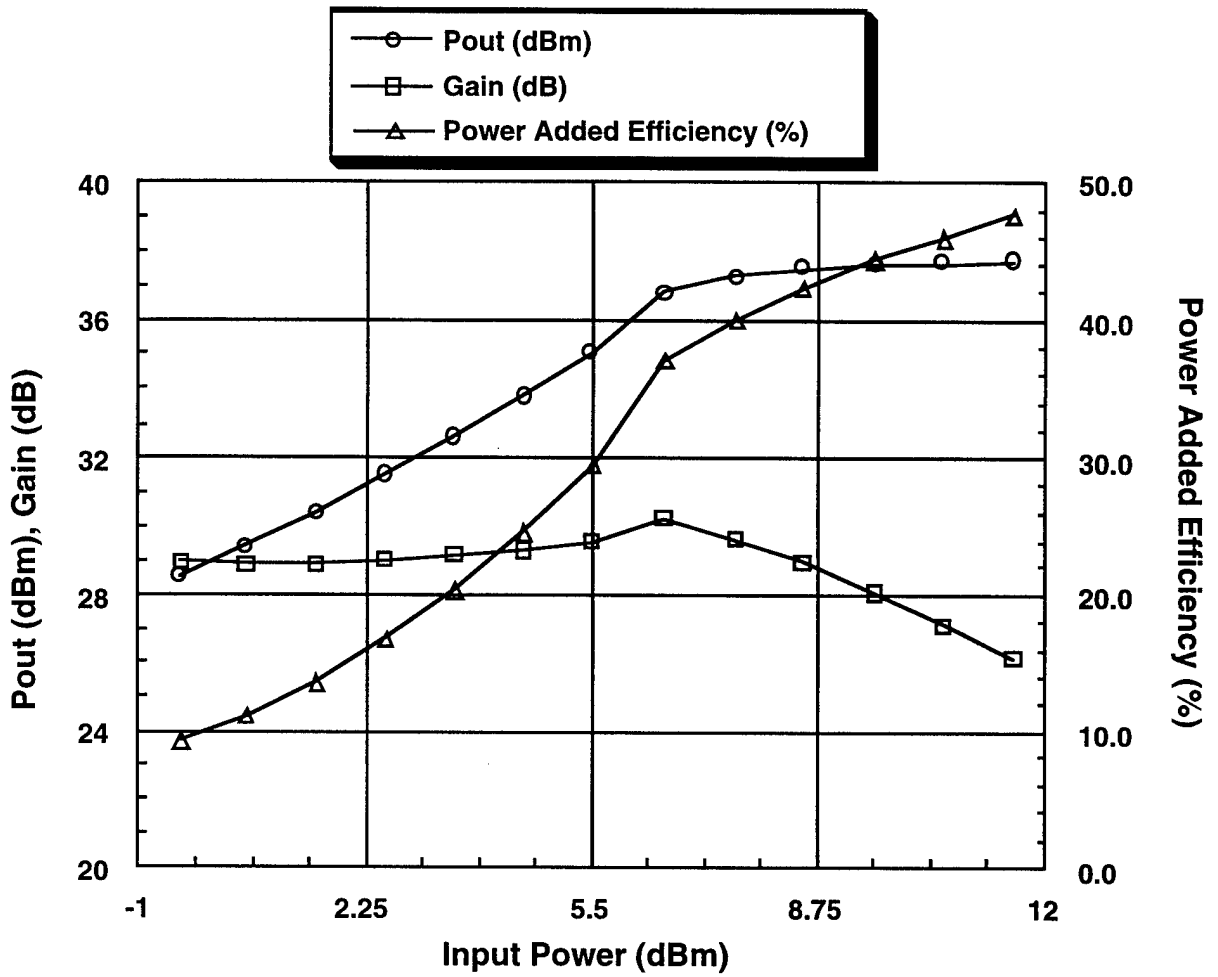


Figure V.7: Performance of a fully assembled C-Band power amplifier in LTCC-M package.

Raytheon is pleased with the performance of this LTCC-M package. Future Raytheon plans for LTCC-M include the demonstration of its applicability for products that operate at millimeter wave frequencies.

3. Lessons Learned

- Exposed wide lines that pass through the seal ring have a tendency to crack during firing. Maximum line width seems to be about 12 mils without further optimization. If wider conductors are required, then several 12 mil lines should be connected in parallel.
- Cuts through fired ceramic should avoid areas where silver contact pads are printed on the metal core. These areas exhibit a much greater tendency to crack during the "sawing" operation.

E. ADVANCED PCMCIA CARDS

1. Design

Torrey Science completed the design of the RF Modem Module and sent the circuit layout data to Sarnoff for substrate fabrication. Some key features of the design are:

- The design is based on an extended PCMCIA Type II card format.
- This is a 2-sided module with digital circuitry on one side of the LTCC-M substrate and the RF circuitry on the other side.
- Interconnections between the digital and RF circuitry are provided by means of insulated feedthroughs in the Cu/Mo/Cu metal core.
- Interconnections within the digital circuitry are provided by means of a 6-layer multilayer construction. The RF side consists of four ceramic layers.
- The design utilizes surface mount devices and packages, bare die (total of 16), and surface mount connectors for external connections.

2. Substrate Fabrication Tooling

Design data from Torrey Science were converted to various fabrication tools at Sarnoff:

- Via punch files were supplied to the tool and die vendor for building dedicated tooling for punching vias in the ceramic tape. A total of five die sets consisting of a blanking die, two via punch and sets for the digital side, and two via punch and die sets for the RF side were fabricated.
- Gerber files of the various layers of circuitry with alignment keys were supplied to printing screen and stencil suppliers.
- Additional layers of artwork (that are not part of the Torrey Science design package) needed for LTCC-M construction, such as glaze layers, contact metal pads layers, and stabilization layers were supplied to the screen vendor.

3. Module Assembly

Torrey Science selected CTM, Microelectronics Packaging, Inc. (San Diego, CA) as the module assembler. Several steps were initially taken to facilitate the assembly process:

- Double-sided solder assembly trials were run at Sarnoff to verify materials-process compatibility. Good results were obtained with eutectic Sn-Ag as the high temperature solder and eutectic Sn-Pb as the low-temperature solder. These test modules were subjected to 125 of -65/+150°C thermal cycles and passed continuity tests and visual criteria.

- Enhancements to the top surface conductor were incorporated for better reliability.
- Double-sided substrates with only top surface metallization were fabricated and provided to CTM during the 4th quarter of 1996. These initial trials did not raise any assembly issues, and assembly tooling was designed and constructed.

4. Substrate Fabrication

About two dozen complete 2-sided substrates, shown in Figure V.8, were fabricated during the course of this program. In June 1996, after several lengthy delays (to be discussed later in this section) Sarnoff was informed by Torrey Science that CTM would no longer be able to assemble the module. As this point, the best substrates still exhibited several shorts to the metal core, and also had 3 to 10 open nets. It was decided to cease building substrates, since they could no longer be assembled or tested.

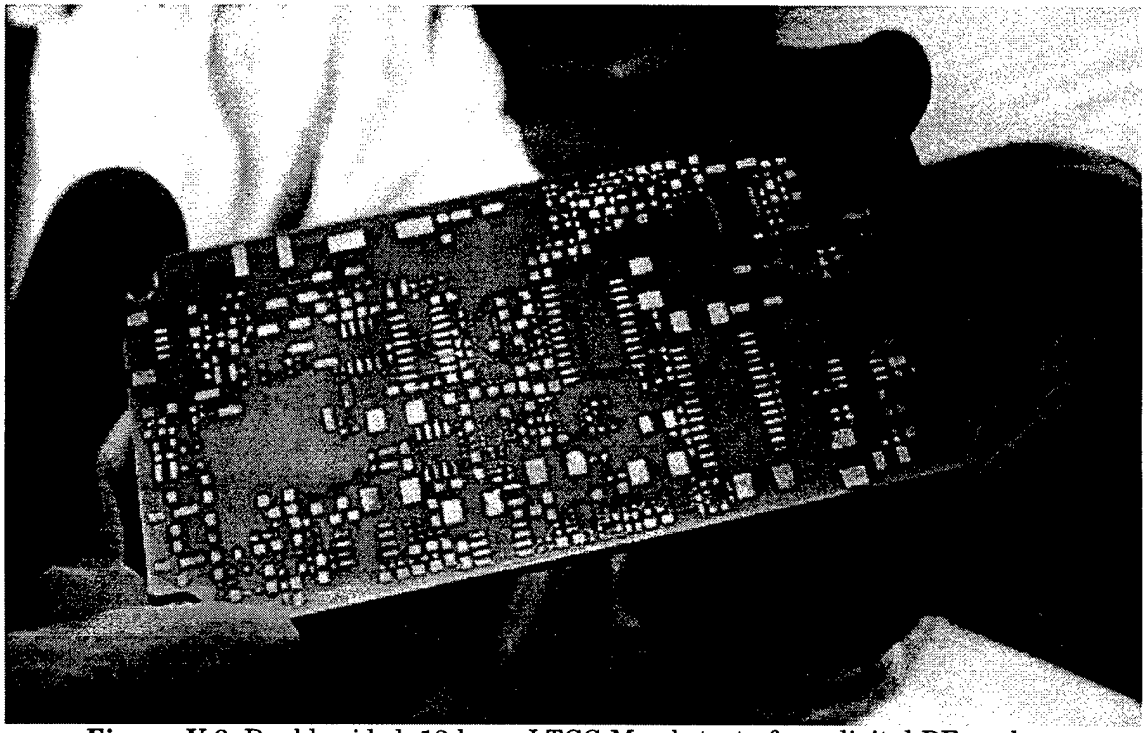


Figure V.8: Double-sided, 12 layer LTCC-M substrate for a digital RF modem.

Problems with substrate design and fabrication

The primary cause of delays to the fabrication of this Technology Demonstration vehicle, lies with the inability of Torrey Science to provide Sarnoff computer generated artwork that was free of artifacts. The AutoCad files supplied to Sarnoff were initially unreadable, and when eventually deciphered, they required more than 1 man month of manual labor just to remove the numerous artifacts in the files. It is believed that these artifacts were generated by the ORCAD layout program that was used to design the substrate. It should be noted that Sarnoff has previously worked with substrate layouts designed using ORCAD, and never observed these artifacts. This extensive manual labor caused

several errors to be incorporated into the artwork that were not discovered until much later in the program. Furthermore, whenever artwork changes were required, the files from Torrey Science always required extensive manual touch-up to eliminate the same types of artifacts. This alone led to several months of delays in this program.

When the AutoCad files supplied by Torrey Science were converted to Gerber files for screen generation, they exhibited a large number of conductor trace constrictions similar to the one shown in Figure V.9. In some cases, the constriction reduced the line width to less than one half of its intended width. It is suspected that some of these constrictions crack during the firing process, leading to the few random opens observed with every substrate. Newer thick film conductor inks were formulated to minimize this problem, but all substrates have shown at least two opens attributed to this failure mechanism. This problem cannot be solved without generating a new substrate layout that does not produce these constrictions, and remaking all conductor trace screens.

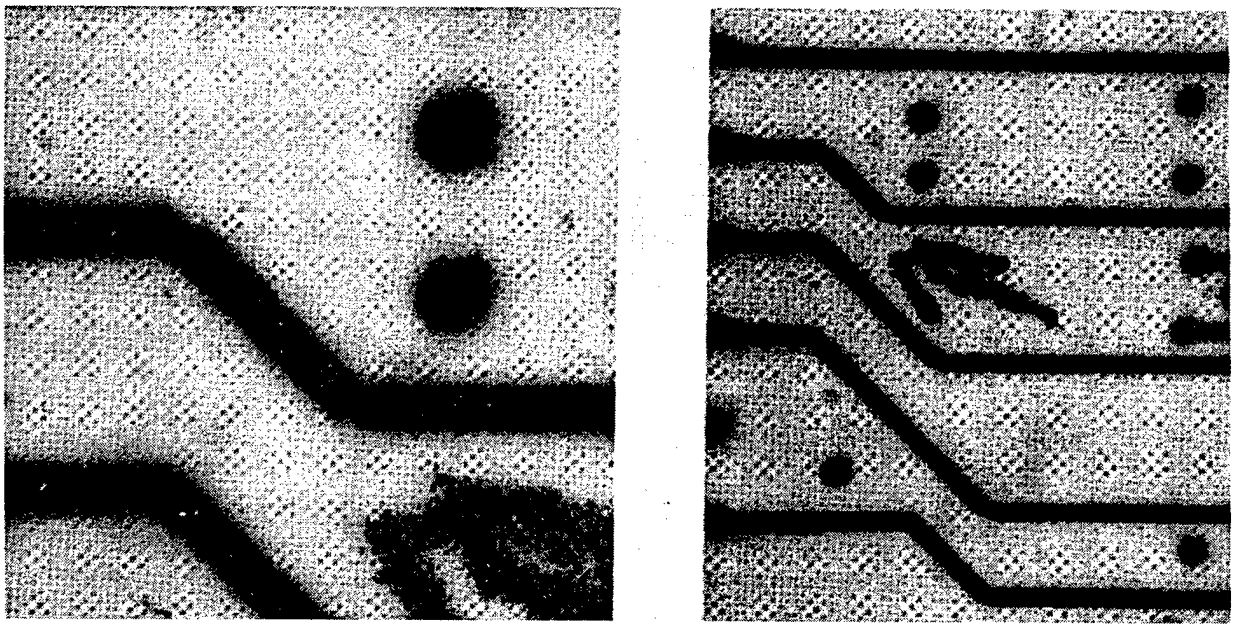


Figure V.9: Conductor trace constrictions due to artifacts in the original AutoCad files supplied for artwork generation.

After the initial group of substrates were built, Sarnoff determined that printing artifacts were causing shorts in the power and ground planes. The primary cause of these artifacts were unnecessary contact pads generated by the ORCAD circuit design software. These pads were generated because they are necessary when building a substrate using printed wiring board technology, and ORCAD is principally used to design printed wiring boards, not co-fired ceramic boards. At Sarnoff's request, Torrey Science redesigned the ground planes and removed all of the extraneous pads. This artwork change largely eliminated the shorts to the power and ground planes.

At this point, it was discovered that the feedthrough insulation of the metal core was allowing some shorts to the metal core. While the cause of this is not known, it has been observed that this particular design produces a much higher

level of very fine cracks in the metal core feedthrough insulation, compared to any other 2-sided metal core design built by Sarnoff. It is suspected that silver is moving down some of these cracks during firing, eventually leading to shorts to the core. New center conductor thick film inks were formulated to solve this problem. First a AgPd(30 wt%) ink was tried. The AgPd ink eliminated the shorting problem, but its contacts to the vias in the green tape were not sufficiently reliable. A Au center conductor was then formulated to eliminate the shorts to the metal core. It is not clear what differences there are between this module and the reliability test structures that were built during Phase 1 of this program. All Phase 1 test structures had many more feedthroughs in the metal core than the present technology demonstration module

Finally, in early 1997 Sarnoff learned that the electroless Ni plating bath (Ni-423 from Technics) that was used to fabricate the Optoelectronic Transceiver Technology Demonstration Vehicle, and was planned for use in this module, was discontinued and no longer available. After considerable effort, Sarnoff developed new electroless Ni plating process, based on the Technics Ni-424 bath.

5. Lessons Learned

1. Difficulties in the procurement of needed components, especially bare dies, led to delays in completing the design by Torrey Science.

2. Design software differences between Torrey Science and Sarnoff continually caused extensive delays in procuring screens. **It is imperative that software designed for layout of multilayer ceramic circuit boards be used**, rather than attempting to retrofit software used to layout printed wiring boards.

3. Holes to align the green tape stack to the metal core should be punched **after** the green tape stacks have been laminated. Holes punched during the green tape blanking operation, can be distorted during the lamination process, resulting in both shorts and opens due to layer misalignment

4. Since green tape can be easily distorted by normal handling, screen printing fiducial holes should never be located near large holes punched in the tape.

5. Au-based thick film inks should be used in the fabrication metal core feedthroughs.

F. POWER ELECTRONIC BUILDING BLOCKS (PEBB)

1. Background

The objective of this task was to design, fabricate, assemble and test a low cost, Transposer (or "lid") for a 200 Watt power switch in support of the U.S. Navy PEBB program, and to meet the packaging needs of high current semiconductor devices. PEBB "lids" are high power device substrates that connect the power device to its control signals on a printed wiring board, and also are part of the thermal management system that draws the heat away from the device (and the printed wiring board). This new PEBB package will eliminate the need for traditional wirebonding for connecting the power device to package external electrodes. This is also a significant improvement over the currently available plastic based power modules that have high parasitic inductive and resistive losses associated with wirebonding. In addition, reliability concerns regarding fatigue of bond wires and fracture of brittle semiconductor die under the stresses of the wirebonding process are eliminated. The total device size was also reduced. The "lid" package was be designed, assembled and tested by Harris Power R & D and fabricated by Sarnoff.

2. Package Challenges

- Prevent camber in the LTCC-M board after cofiring with 0.005" Cu-Mo-Cu metal core and six layers of glass ceramic tape.
- Accommodate very high density of vias over a large portion of the LTCC-M board, resulting from inherent design and multi-up of parts in a single board.
- Achieve good via contact through six layers of glass ceramic tape down to the metal core.
- Prevent cracking of the glass ceramic and cracks in the via material itself throughout the entire LTCC-M board.
- Devise and optimize the process for patterning the 0.005" Cu-Mo-Cu metal core by etching.
- Achieve surface conductors having excellent solderability and adhesion for attachment of bare power die.

3. Initial Module Fabrication

The final design of the package (unit cell) is shown in Figure V.10 with the modified dimensions, this is an X-ray view of the entire package. All of the 0.008" vias in the larger pads are on 0.024" centers. Two hundred of these packages were delivered to Harris Power R&D for assembly and evaluation.

The dimensions of LTCC-M packages for Cu-Mo-Cu were optimized on a 3" x 3" metal core. The PEBB package design called of a 0.400" x 0.600" package. This provided an opportunity to multi-up the number of such packages per LTCC-M board. It was determined that a 3 x 4 array of packages per board would be optimal.

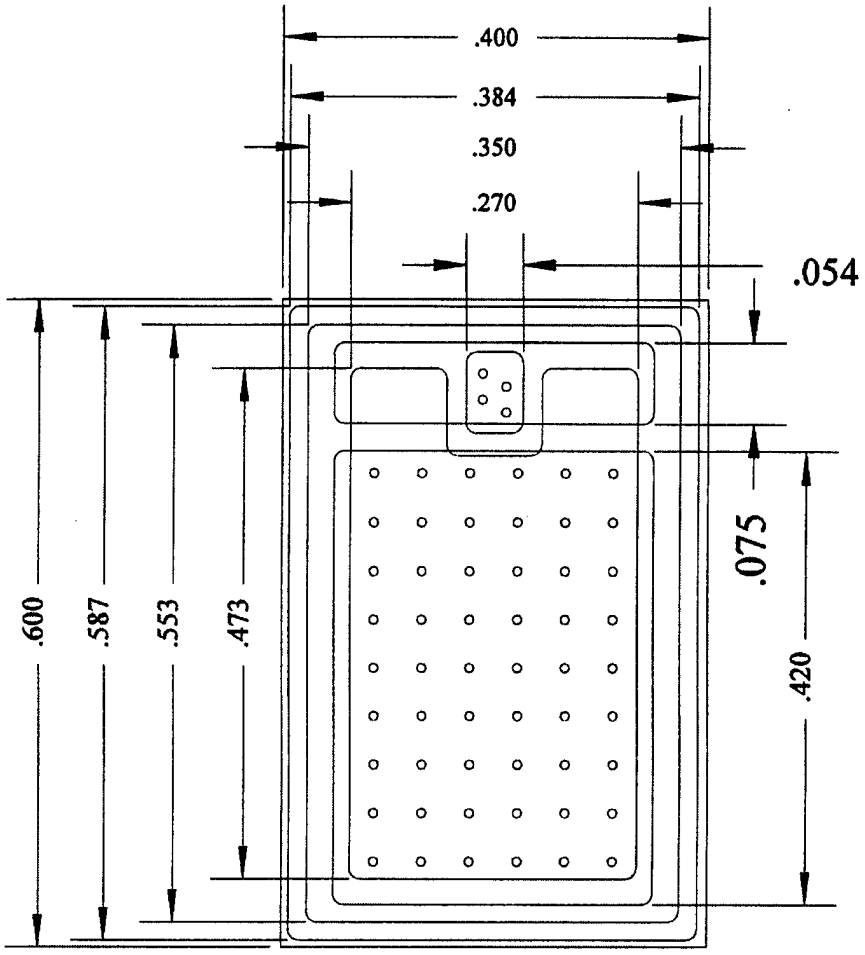


Figure V.10: Design of PEBB power switch transposer

Twelve packages per board called for an extremely large number of vias (710 in total, 696 for twelve packages and 14 for fiducials). In addition to such a high via density, all of the vias had to make contact from the top of the thick film AgPd conductor pads down to the Cu-Mo-Cu metal core going through six layers of green ceramic tape (to get a cofired thickness of the glass ceramic above 0.025"). The adaptations of the materials system needed to achieve this task are briefly described below.

Tape Formulation: Six layers of ABT-52 tapes fired on a 0.005" thick Cu-Mo-Cu metal core did not minimize camber to acceptable levels. This called for a modification of the green tape formulation. The "new" green tape formulation (ABT-61) slightly adjusted the component levels of the ABT-52 formulation. Six layers of ABT-61 tapes colaminated onto 0.005" Cu-Mo-Cu metal cores gave "flat" fired LTCC-M boards necessary for preparing the multi-up PEBB packages.

Vias: Punching 710 vias per tape and hence 4260 vias per LTCC-M board (six such tapes per board), and deliver all packages from about 18 such boards, one by one, would be an enormously tedious process. It was therefore decided to design a hard punching tool which will allow punching of all 710 0.008" diameter vias in one step in green ABT-61 tape. The tool was fabricated by an external vendor.

Via filling with Ag-based inks in the ABT-61 green tapes punched by the hard tool was accomplished very successfully. Via ink (VIA 253) designed for this purpose gave excellent results, **over 35,000 vias were filled (50 punched tapes) without a single miss in a single printing session.** This excellent result is owed to a combination of the better quality of vias punched in a single step process and the optimized formulation of the via ink.

A test board of the vias was fabricated in order to assess electrical continuity. A regular (0.020" thick) Cu-Mo-Cu metal core dotted with MC-4 silver ink (prepared earlier in the program) before Ni oxidation, was colaminated with a stack of six ABT-61 tape layers with filled vias and then cofired, see Figure V.11. Each and every of the 696 vias were tested for electrical continuity, and every one of them gave satisfactory results.

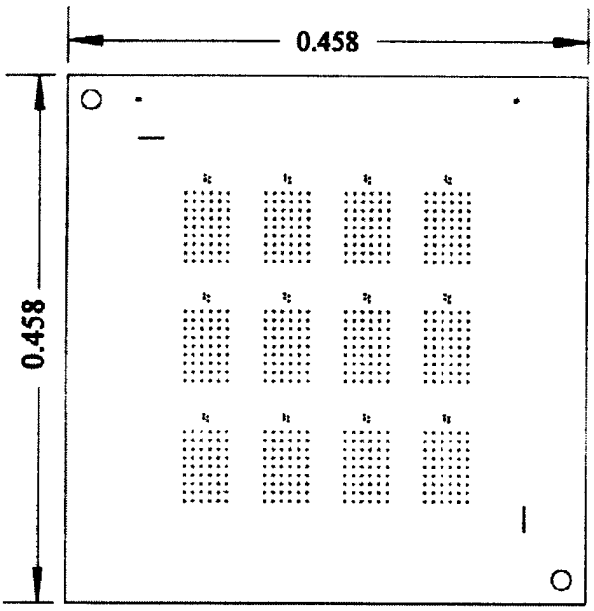


Figure V.11: Via pattern for 12-up layout of PEBB "lid"

Metal Core Preparation: Cutting 3" x 3" 0.005" thick Cu-Mo-Cu metal core by shearing (normal procedure) imparts inherent camber in the metal core, some of which is retained after cofiring. To further minimize camber (in addition to the ABT-61 formulation), the metal cores were cut by wire EDM. There was also a separate challenge to be met regarding perfect alignment of the metal core to the green tape laminate during colamination. The traditional optical technique used for colamination developed earlier in the program for via contact to metal did not have sufficient tolerance to align the very large number of vias in this prototype. It was determined that colamination had to be carried out in the Cu fixture itself that is also used for green tape stack laminations. To accomplish this, two holes (along the diagonal) were added to the metal core to mate with the alignment pins. Also two separate holes along an edge added to the metal core for high resolution optical alignment for photoresist deposition on the backside. All of these holes were drilled and then smoothed by wire EDM to 0.004" mil oversize in diameter to allow for Ni plating. To minimize waste, the Cu/Mo/Cu metal core (13" x 13" as received) was cut to 2.75" x 2.75" instead of 3" x 3".

The multi-up board with 710 0.008" diameter vias on 0.024" centers would minimize the amount of bonding glaze delivered to individual parts. After a few combinations of gaps in the bonding glaze, the optimum size of the opening in the glaze was determined to be a 0.016" square pattern on 0.024" centers and with the same centers as the vias. In order to minimize stresses in the firing of the glaze, a 0.010" gap (channel) was provided exactly in the middle of all the twelve individual parts. After etching of Cu-Mo-Cu, this conveniently served as cutting

keys for singulation. However, to print the glaze in such a sharp pattern, an especially viscous inkhad to be formulated.

The metal core preparation included the steps of silver dotting the metal core after Ni plating with MC-4 ink using a stencil which had 0.012" squares at the same centers as the vias. This was followed by firing the ink to the metal core. This was followed by printing and firing the glaze. BC-103 silver was then dotted using the via stencil and then dried.

Lamination & Colamination : Six layers of ABT-61 with all the vias punched and filled (with Via 253 ink) were stacked. The top conductor pattern was printed on the top tape in the stack with a newly formulated top conductor ink TC-9. The bottom side of the bottom most tape of the stack (one which comes in contact with the metal core) was dotted with BC-103 with a stencil designed to do so. A tape of LN-1 was placed on the top of this six layer stack. Lamination was carried out using standard Cu fixtures at 3,000 lbs. load for a total of 2 min. after a 1 min. preheat at 185°F. Colamination was done by first putting the metal core in the fixture and then putting the laminate on top of it in the same fixture at 600 lbs, also for a total of 2 min. after a 1 min. preheat at 185°F. Shearing was done after colamination to remove 0.125" from around each edge of the laminate. The part was then cofired and LN-1 tape washed off.

Gold Plating & Etching : A cofired part with LN-1 washed off was first subjected to standard nickel oxide stripping. The back side of the part, *viz.*, the exposed Ni side, was covered with a photoresist to develop a pattern for Au plating corresponding exactly to the etched pattern of Cu-Mo-Cu. A mask was designed to do so, such that after the photoresist deposition, Au was deposited by electroplating on both sides, the thick film and the Ni on Cu-Mo-Cu side was covered with gold corresponding exactly to the top and bottom pattern of the PEBB package. The Au on the metal core side can act as an etch mask by itself. However, in doing so there was significant undercutting during the etching process (up to 0.012"). This problem was minimized by designing an over-sized photo mask. Using this mask the photoresist was deposited on the electroplated Au on the metal core side and then the part was etched. The etching process was optimized to etching at 70°C for just under 5 min. The etchant was a mixture of HCl, HNO_3 and H_2SO_4 diluted with distilled water.

Singulation : The dicing of the individual twelve parts from the etched LTCC-M boards involved mounting them on a plate by waxing and cutting using a 0.015" thick blade. The cutting keys were already present by design of the glaze screen. After cutting, the parts were washed with organic solvents to clean off the wax. The entire singulation process was relatively rapid. Figure V.12 illustrates the two sides of a finished package.

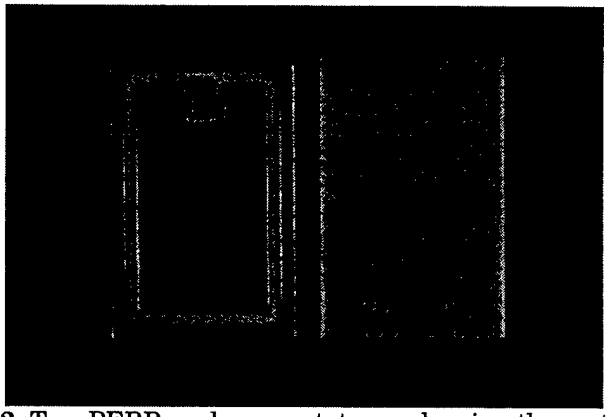


Figure V.12: Two PEBB package prototypes showing the metal patterns.

4. Second Iteration Module Fabrication

Sarnoff supplied Harris with a more than 200 "initial design" PEBB "lids". During assembly of these modules by Harris, it was discovered that the adhesion and solderability of the AgPd was insufficient to meet the Harris specifications. The design was revised to eliminate the cofired top conductor, and to have the top conductor layer plated and etched, prior to package singulation. Since the top conductor was deposited after the ceramic firing step, it was no longer cost-effective to pattern the Cu/Mo/Cu by etching; instead the metal core was eliminated. Utilizing LN-1 tapes on the top and bottom of the green tape stack allowed the glass/ceramic to be fired without any shrinkage.

Sarnoff delivered "second iteration" packages to Harris Power R&D as multi-up "wafers.' These "wafers" were then sent to Titanium Finishing for plating, then returned to Harris for spray etching, and finally sent back to Sarnoff for singulation. 150 packages were delivered to Harris for assembly and evaluation.

5. Package Evaluation

Harris never provided Sarnoff with a written evaluation of these packages. However the verbal evaluation provided by Harris personnel for the "second iteration" packages were:

- excellent solderability of the plated conductor
- excellent adhesion of the plated conductor to the LTCC-M ceramic
- highest thermal conductivity of any "lid" made with any packaging technology (This is due to the use of high conductivity silver vias, and because LTCC-M allows a higher density of thermal vias in the "lid".)
- very low inductive loss (Again, this is due to the higher density of vias allowed by cofired green tape technology.)

6. Lessons Learned

- One should not attempt to form large area conductors by a single screen printing operation. Large area conductors tend to print much thinner than typical conductor traces, since the emulsion cannot support the screen mesh in the center of the pad. As was observed during the Technology Transfer to DLI, thinly printed top conductors exhibit much poorer adhesion to the LTCC-M glass/ceramic. Therefore multiple

screen printing steps, or use of a post-fired layer printed on top of a cofired pad is necessary.

- For high solderability surfaces, LN-1 layers must be cleaned more thoroughly, than by simply scrubbing in water. Use of a sand abrasion technique, such as the one in use at DLI is recommended. Such surfaces can be readily electroplated with highly solderable metals if desired.
- Etching the Cu/Mo/Cu base of LTCC-M weakens the ceramic to metal bonding layer.

Section VI
Important Findings and Conclusions

A. INTRODUCTION

A low loss, ceramic-on-metal substrate technology matched to GaAs has been developed for interconnecting bare die (either silicon or GaAs) as well as passive components. This technology is also suitable for fabricating hermetic single or multichip packages for a wide variety of military and hi-rel commercial applications. The combination of a low loss ceramic at microwave frequencies and a high conductivity metal core makes LTCC-M a natural choice for substrates and packages for advanced communication systems and mobile computing. All major technology elements, shown in Table VI.1, of a double-sided circuit board capable of interconnecting MCMs, bare die, flip chips, packaged ICs (surface mount), and passive components were developed and demonstrated by the Sarnoff Corporation. Electrical feedthroughs in the metal core provide a minimum length interconnect between the top and bottom sides of the circuit board. The LTCC-M circuit can also serve as the power and ground planes for high density MCM-D signal layers. This reduces the number of MCM-D layers, resulting in a lower cost for such a module. Benzocyclobutene (BCB) test structures with nominal features sizes as small as 1 mil were fabricated on top of polished LTCC-M substrates to demonstrate this capability. During this program, 4 prototype circuits (each emphasizing a different attribute of LTCC-M) were designed and fabricated to prove out the technology. Three of these were completed and delivered to the supporting company as fully tested bare substrates. All of these substrates were favorably reviewed, especially the microwave power amplifier prototype.

While the technology demonstration vehicles showcase qualities required for compact, high functionality military systems, they also support the creation of high volume products for the commercial marketplace. Typical military applications include: personal units for cellular communications systems and wireless LANS, electronics for tracking of military materials and components, construction of affordable broadband networks at military bases and installations, T/R modules for radar systems, and high power motor control systems. Specific military systems to which LTCC-M substrate technology can be applied include: Global Mobile Information Systems (US Army), "Total Asset Visibility," Power Electronic Building Blocks (US Navy), EKV Program (US Air Force), and the AEGIS Radar System (US Navy).

Table VI.1: Major LTCC-M Elements Demonstrated During This Program

Low Cost Feedthrough Process
- Hole fabrication by laser or mechanical drilling
- Hole insulation
- Center conductor

Green Tape Development
- Glass/ceramic
- Low loss ceramic
- CTE of glass/ceramic matched to Cu/Mo/Cu
- Green tape formulation

Ceramic to Metal Bonding
- Cu/Mo/Cu surface preparation
- Glaze development
- "Zero" lateral shrinkage

Conductor Development
- Buried silver conductor
- Via silver conductor
- Exposed Ag/AgPd conductors

Multilayer Integration
- Double-sided board fabrication and firing
- Precision cavity formation process

Thin Film Process
- Thin film conductors on glass/ceramic
- BCB processing
- Thin film multilayers on LTCC-M

B. LTCC-M TECHNOLOGY DEVELOPMENT

The LTCC-M system has been developed for use with a Copper/Molybdenum/Copper clad metal laminate. This low expansion, high thermal conductivity core **allows direct mounting of high power silicon or GaAs bare die**, while allowing the designer **flexibility in thermal management system design**. The green tape is a crystallizing glass-ceramic designed for a thermal expansion match to the Cu/Mo/Cu core. Under this contract, materials and processes have been developed to bond the ceramic to the metal core during the firing step, such that the **ceramic does not shrink in the lateral (x,y) plane**. However, the glass-ceramic achieves full densification by shrinking in the z-direction. Zero shrinkage is critical for mating cofired ceramic circuits to a metal core having electrical feedthrough vias. Furthermore**, zero shrinkage allows LTCC-M to achieve large area format processing, which is essential for low cost production**.

Materials and processing for mass fabrication of many small electrical feedthrough vias in the metal core have been developed under this contract. Holes as small as 7 mils in diameter have been laser drilled in 20 mil thick Cu/Mo/Co cores, conventional drilling can produce 13 mil diameter holes. Screen printing techniques are then used for forming coaxial feedthroughs for interconnecting circuits formed on the top and bottom sides of the circuit board.

Significant LTCC-M materials system accomplishments during this program include:

- Demonstrated low loss, 50Ω transmission lines with seal ring feedthroughs; 50Ω lines were **tested to 20 GHz and exhibited low loss** (<0.25 dB/feedthrough, and <-15dB return loss) throughout this frequency range.
- Demonstrated thick film spiral inductors from 5 - 30 nH that agreed with model calculations, and had self resonant frequencies up to 4.5 GHz
- Developed process to form **high precision cavities (<1mil tolerance)** in LTCC-M substrates.
- Development of a series of Ag and AgPd thick film top conductor inks (compatible with electroless Ni/Au plating) that exhibit good adhesion to the LTCC-M ceramic; and can withstand more that 600 thermal cycles between -55°C and +125°C, without any loss of adhesion.
- Development of a set of thick materials that can produce high density substrates having 4 mil lines and spaces with 4 mil diameter vias in the ceramic; daisy chain structures have withstood 600 thermal cycles between -55°C and +125°C.
- Temperature humidity studies at 85°C, 85%RH, 48 volts (>3000 hours) **show no evidence of silver migration** through the glass-ceramic.
- Daisy chain test structures have been fabricated in LTCC-M ceramic having 8 mil lines, spaces and vias. These test structures have undergone more than 250 thermal cycles between -40°C and +125°C, without any change in electrical resistance or any visible signs of via cracking.

C. TECHNOLOGY TRANSFER TO A MERCHANT SUPPLIER

An LTCC-M **Technology Transfer program was successfully completed with Dielectric Laboratories Inc.** (Cazenovia, NY). Dielectric Laboratories will be a merchant supplier of LTCC-M packages and substrates to both military and commercial electronics systems manufacturers. A goal of this program was to replicate the LTCC-M processing at Dielectric Laboratories and its chosen suppliers. **During this program all custom glasses, silver thick film inks, and green tape were transferred to commercial sources for scale-up to commodity sized lots**; the LTCC-M components were reformulated to account for differences of the purchased materials, and processing was adjusted to accept these changes. The Technology Transfer was concluded with the fabrication and delivery of 20 C-Band Power Amplifiers by Dielectric Laboratories.

D. TECHNOLOGY DEMONSTRATION VEHICLES

- 30 Optoelectronic Transceiver Packages were delivered to AMP for a 1.2Gbit/sec Fiber-in-the-Loop system. These packages were built with a **90% first pass yield**.
- 15 C-Band Power Amplifiers were delivered to Raytheon. The package was demonstrated to handle 38 dBm of output power at efficiencies greater than 45%, and **these amplifiers met all specifications**.
- 350 Transposers for a 200 Watt power switch were delivered to Harris for the US Navy Power Electronic Building Block Program. These transposers demonstrated **very low inductive losses** as well as **excellent thermal conductivity**, critical properties for high power electronic modules. Their superior thermal properties are a result of the fact that low temperature

cofired ceramic substrates offer a much higher via density coupled with high conductivity silver vias, compared to conventional alumina substrate technology.

- A Digital/RF Modem in 2-sided PCMCIA Card Format was also fabricated during this program. While no board passed bareboard test without any defects, it is expected that all problems can be readily fixed. This Technology Demonstration Vehicle was discontinued primarily due to the substantial delays encountered during substrate fabrication. The most important cause of these delays were incompatibilities between the design files generated by Torrey Science (using ORCAD design software) and the AutoCad software in place at Sarnoff. The design files contained numerous artifacts, some of which were manually removed from the files in a very labor intensive manner, but the circuit constriction artifacts could not be removed without completely laying out the circuit again. **An important lesson learned from this task, is that the substrate design software must be developed for the substrate fabrication technology.** ORCAD is primarily a printed wiring board layout tool, and it was "forced" to lay out a cofired ceramic board that relied on a totally different fabrication process. The incompatibility between design files and the substrate toolmaking software led to both errors and significant delays.

Section VII
Significant Developments

A. LTCC-M MARKETING EFFORT

During the course of this technology transfer effort DLI made significant contributions, above the requirements of this program, to demonstrate their interest in establishing this technology in the market place. DLI had an independent marketing analysis prepared by Prismark Associates to help identify both the market that DLI should target, and the size of the market that they should expect. In June 1997, DLI introduced LTCC-M technology to potential customers and to their reps at the IEEE MTTS show in Denver, CO. At this show DLI also presented a paper on LTCC-M technology. This effort generated much interest from potential customers in the areas of high frequency and high thermal power applications. The aspect of low cost was also considered to be a technology driver. Since then DLI has had discussions with numerous potential customers such as Raytheon, AMP, Hughes, Litton, Alcatel and Ortel. DLI has also discussed the technology with two sister companies, CTI and Vectron, and is currently building packages for CTI to evaluate. A purchase order from Raytheon to build an amplifier package has also been received. Finally, DLI has been approached by Sarnoff, TRW and Harris to determine if their is interest in partnering on other government proposals. DLI has submitted a quote to TRW to fabricate two MCMs for the DARPA Digital Radar program.

Internally DLI has developed a cost model for LTCC-M, and has prepared and distributed a capabilities brochure and preliminary design guideline for this technology. They are also working on a WEB site to insure that information on this technology is easily attainable. All LTCC-M manufacturing will be done in a new 5000 square foot facility that has just been completed.

B. LIST OF PATENTS FILED

Inventors	Title
Kumar, A.H., Thaler, B.J., Prabhu, A.N.. Tormey, E.S.	Low Loss Dielectric Glasses
Azzaro, T.P., Thaler, B.J., Conlon, E.J., Kumar, A.H.,	Electrical Feedthroughs for Ceramic Circuit Board Support Substrates
Prabhu, A.N., Thaler, B.J.	Glass Bonding Layer for Ceramic Circuit Board on Support Substrates
Kumar, A.H., Thaler, B.J., Prabhu, A.N., Tormey, E.S.	Conductive Via Fill Ink for Ceramic Multilayer Circuit Board on Support Substrates
Sreeram, A.N., Thaler, B.J., Prabhu, A.N.	Technique to Control Cavity Dimensions and Lipping in LTCC-M

Section IX
Future System Extensions

The LTCC-M system will be extended to integrate passive components into the substrate under DARPA contract # F33615-96-2-5105. Materials to screen print capacitors and resistors on the LTCC-M green tape layers will be developed and transferred to Dielectric Laboratories Inc. Besides resistors and capacitors, inductors and filters can be formed within the substrate. Design kits will also be developed to aid system designers in using this new substrate technology.

The large area capability of LTCC-M opens up new horizons for the use of ceramic substrates. Such areas include flat panel displays and phased array antennae where the control electronics are integrated with the display or antenna. A DARPA sponsored program is underway to develop and demonstrate technology for integrating electroluminescent displays with related electronics on high-performance circuit boards. The LTCC-M multilayer circuit board technology is being adapted for this purpose. Planar's atomic layer epitaxy (ALE) process is used to form EL stacks on top of the LTCC-M substrates. Following development and demonstration of critical materials and processes, a sample 3" x 5" display with integrated drive electronics will be fabricated. CDC will assemble this display into a vehicle display system for demonstration to the military. In addition to providing smaller and simpler display packaging by integrating drivers onto the display and by using a robust ceramic-on-metal display panel, this technology will improve display brightness and efficacy by addressing the EL display in multiple segments with conductive vias through the circuit board and by improving component thermal dissipation. In the long term, this technology forms a basic building block for supporting new display functionality by enabling the integration of sensors, communicators, processors, etc. onto the display panel.

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This is the final progress report for the Ceramic Metal Composite Circuit-Board-Level Technology for Application Specific Electronic Modules (ASEMs). This report summarizes the entire research program. Areas included in the report are: LTCC-M Materials System Development, Technology Transfer to Dielectric Labs, Inc., Fabrication and Evaluation of the Four Technology Demonstration Vehicles, and Future Extensions of the LTCC-M Technology.

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